
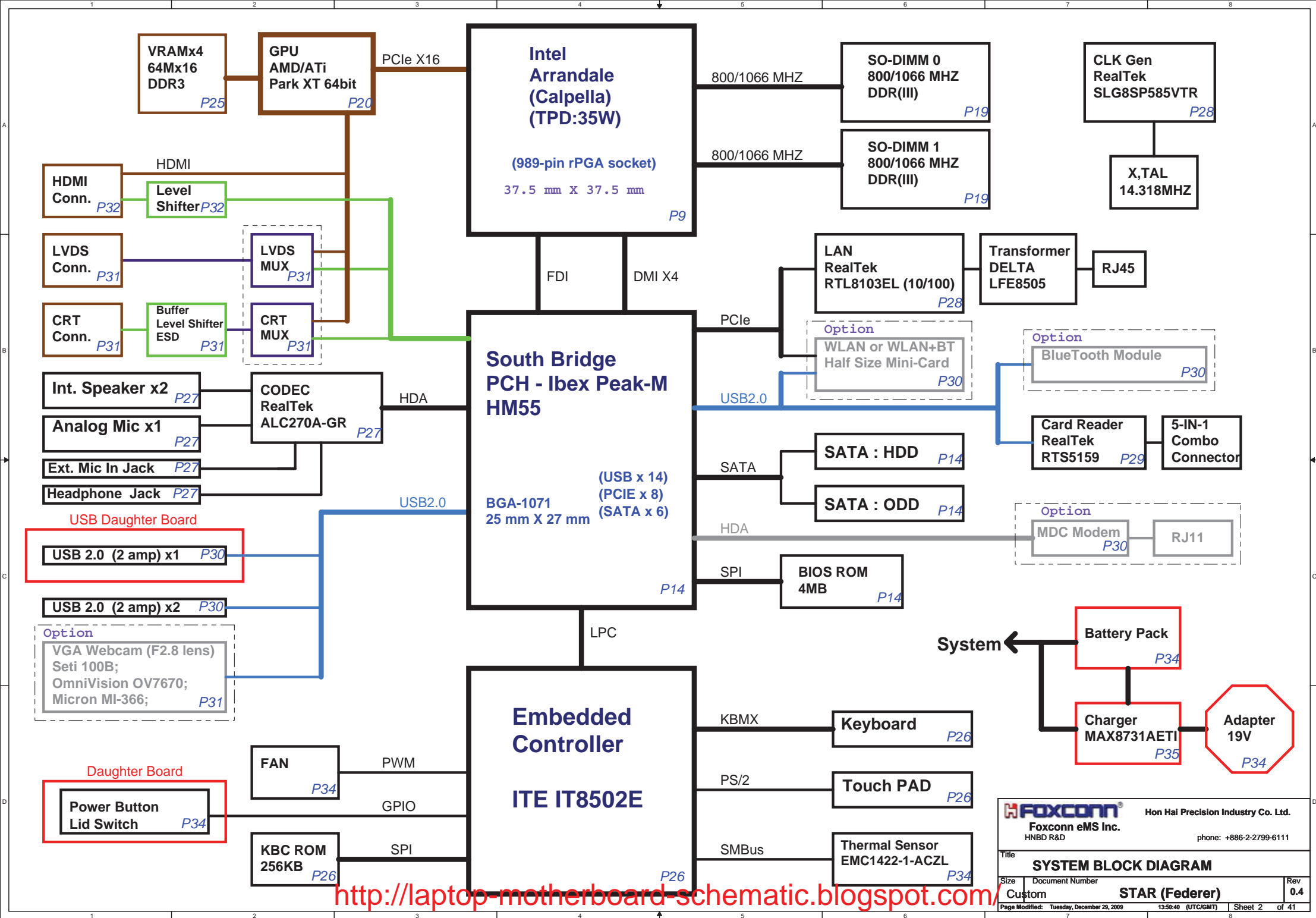
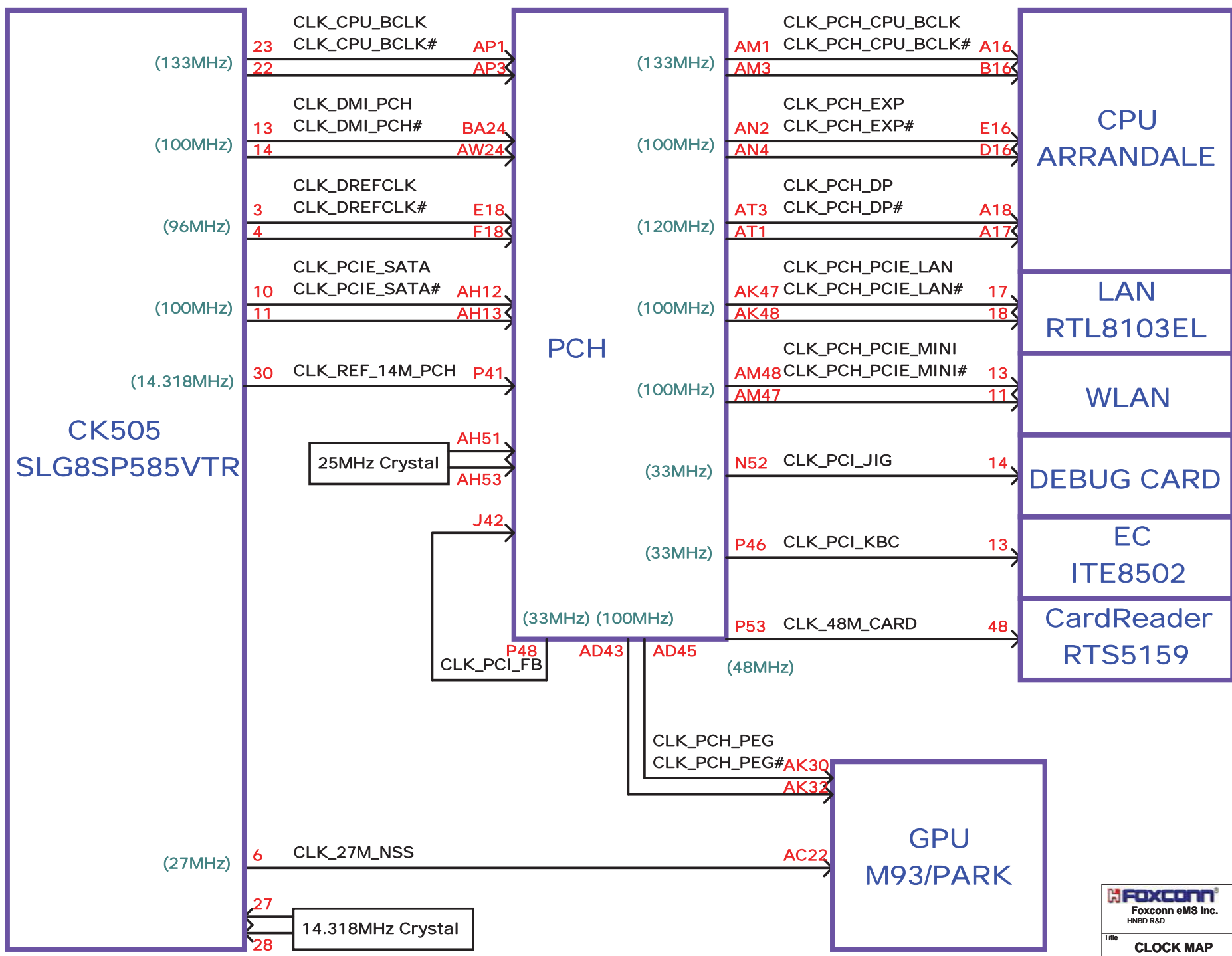


01 -- COVER SHEET	21 -- VGA_S3 (IO) 2/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DDR3) 3/5
03 -- CLOCK MAP	23 -- VGA_S3 (DP) 4/5
04 -- POWER MAP	24 -- VGA_S3 (POWER) 5/5
05 -- POWER SEQUENCY DIAGRAM	25 -- VRAM (DDR3)
06 -- POWER SEQUENCY TIMING	26 -- EC+KBC (IT8502E)
07 -- SMBUS MAP	27 -- CODEC/JACK/SPEAKER/MIC
08 -- RESET SIGNAL MAP	28 -- LAN (RTL8103EL)/CLOCK GEN
09 -- Calpella (DMI,PEG,FDI)	29 -- Card Reader
10 -- Calpella (CLK,MISC,JTAG)	30 -- WLAN/BT/MDC/USB/MOUNTING
11 -- Calpella (DDR3)	31 -- LVDS/CRT/Webcam
12 -- Calpella (POWER/GND)	32 -- HDMI
13 -- Calpella (GRAPHIC POWER)	33 -- DCIN/Battery/OCP/FAN
14 -- PCH (HDA,JTAG,SATA)	34 -- PWR_Charger MAX8731AETI
15 -- PCH (PCI-E,SMBUS,CLK)	35 -- 5V/3.3V SN0608098RHB
16 -- PCH (DMI,FDI,GPIO,LVDS)	36 -- Vcore MAX17030
17 -- PCH (PCI,USB,NVRAM,GPIO)	37 -- 1.1V VTT/+V1.05RUN
18 -- PCH (POWER)	38 -- 1.5VDDR3+0.75V+V1.8RUN
19 -- DDR3(SO-DIMM_0&1)	39 -- PWR_Others power plane
20 -- VGA (PCI-E/STRAP) 1/5	40 -- CPU VREG & Decoupling
	41 -- ATVDD/+VPCIE

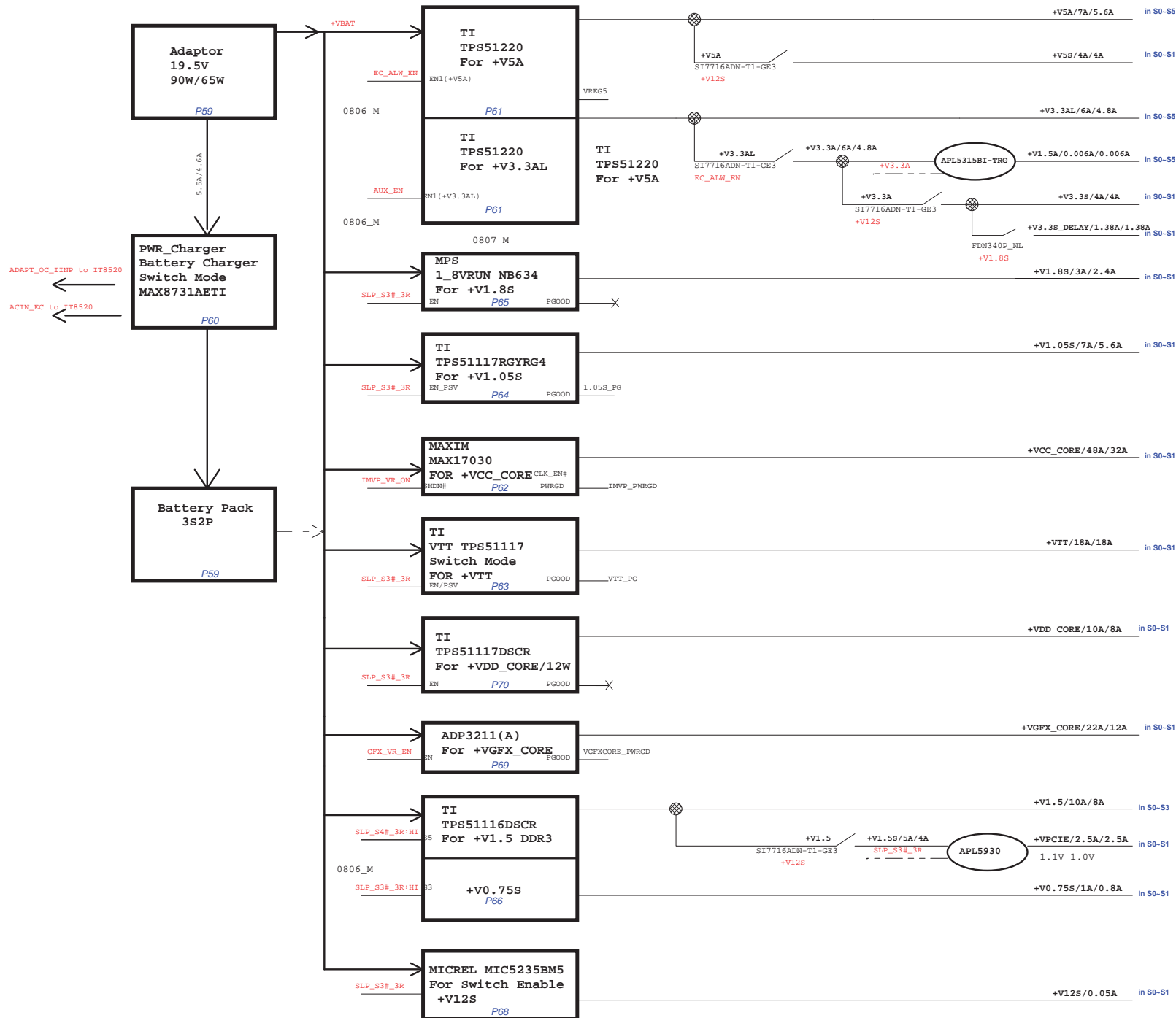
P. Leader	Check by	Design by

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Foxconn eMS Inc.		phone: +886-2-2799-6111	
HNBD R&D			
Title			
Index Page			
Size	Document Number	Rev	
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POWER SEQUENCY DIAGRAM

	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V	V	
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V	V	
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

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FOXCONN
Foxconn eMS Inc.
HNBD R&D

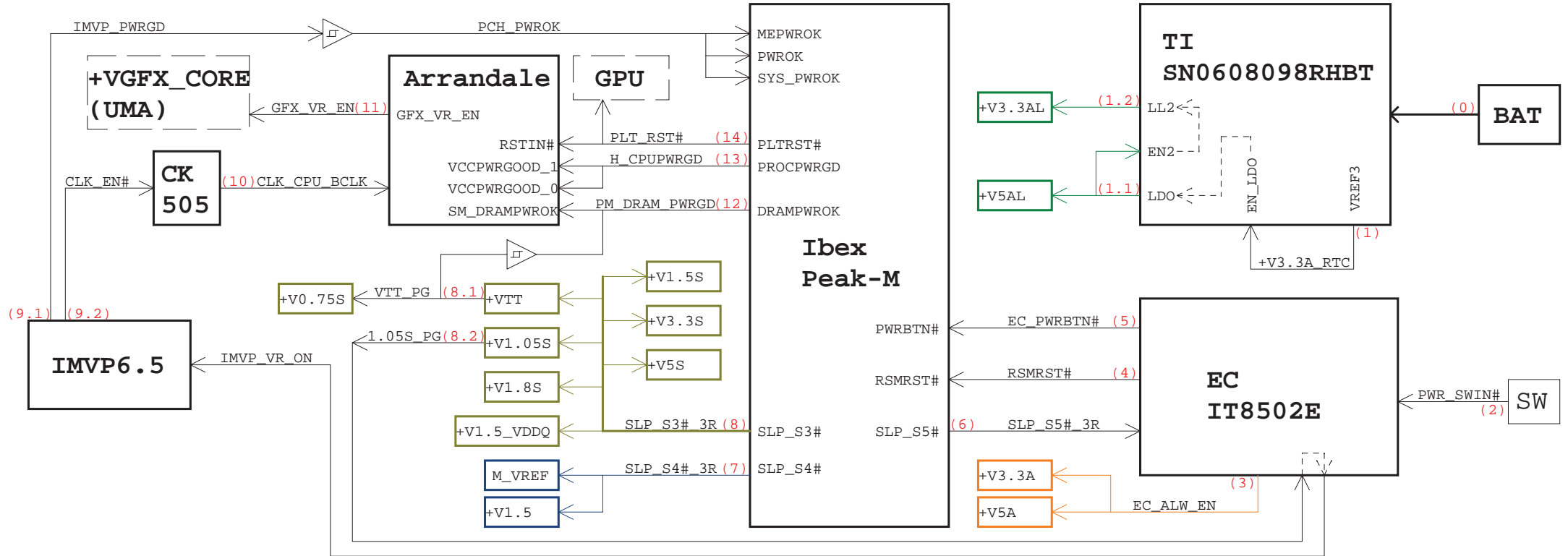
Hon Hai Precision Industry Co. Ltd.
phone: +886-2-2799-6111

Title
Size
Document Number
Custom

POWER SEQUENCY DIAGRAM
STAR (Federer)

Rev
0.4

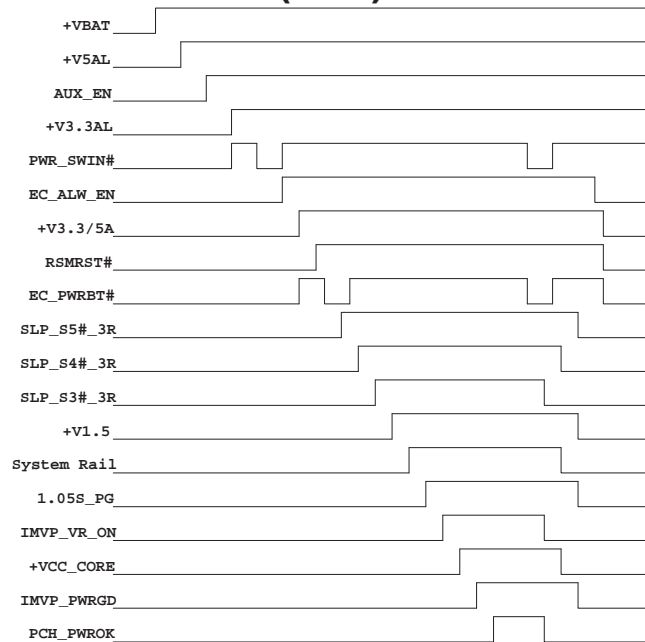
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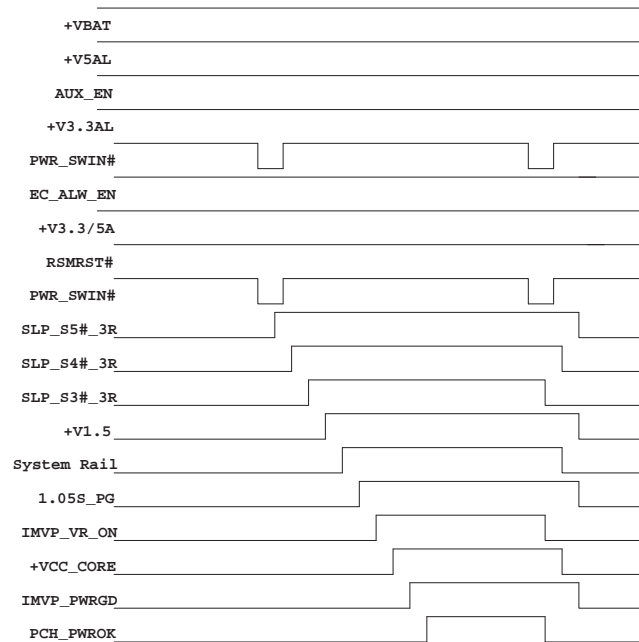
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

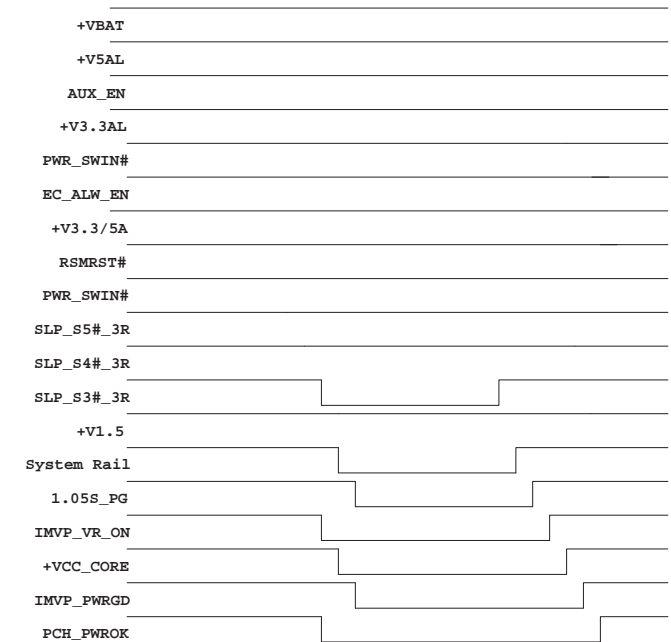
G3(OFF)->S0->S5



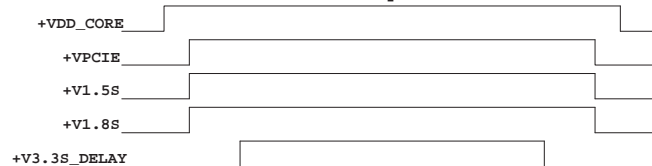
S5->S0->S5



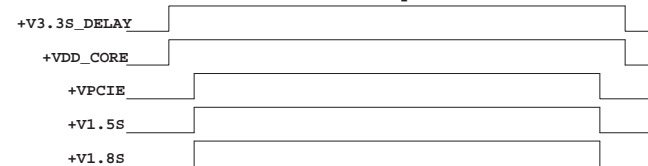
S0->S3->S0



M93 Sequence



Park Sequence



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SMBUS&I2C MAP

Discrete
GPU

GPU
M93/Park
S3 Package

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN

WLAN

Temp
Sensor


Charger

Battery

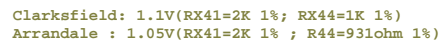
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RESET SIGNAL MAP

<http://laptop-motherboard-schematic.blogspot.com/>

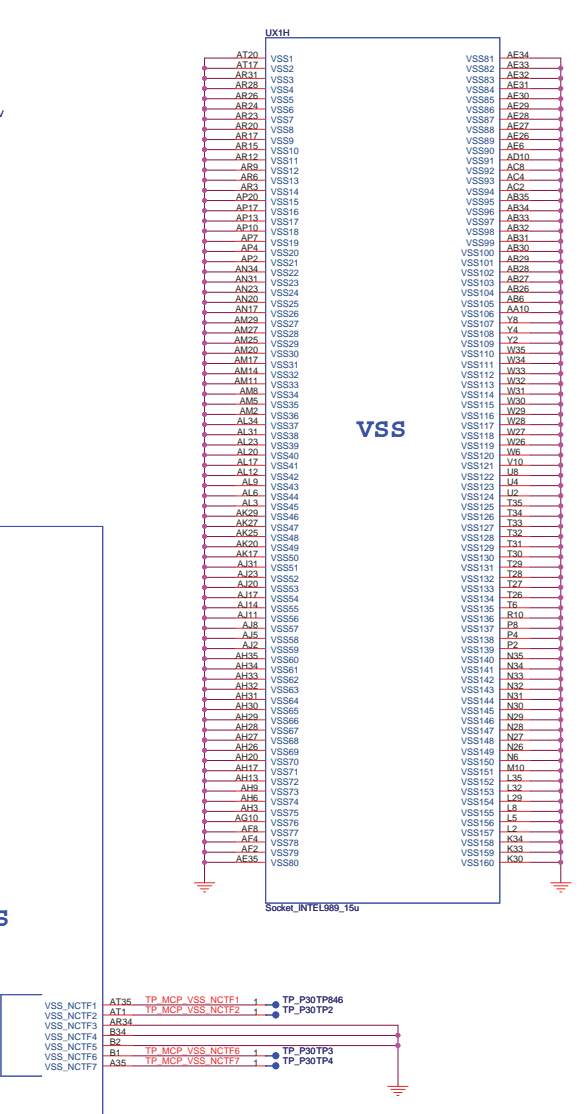
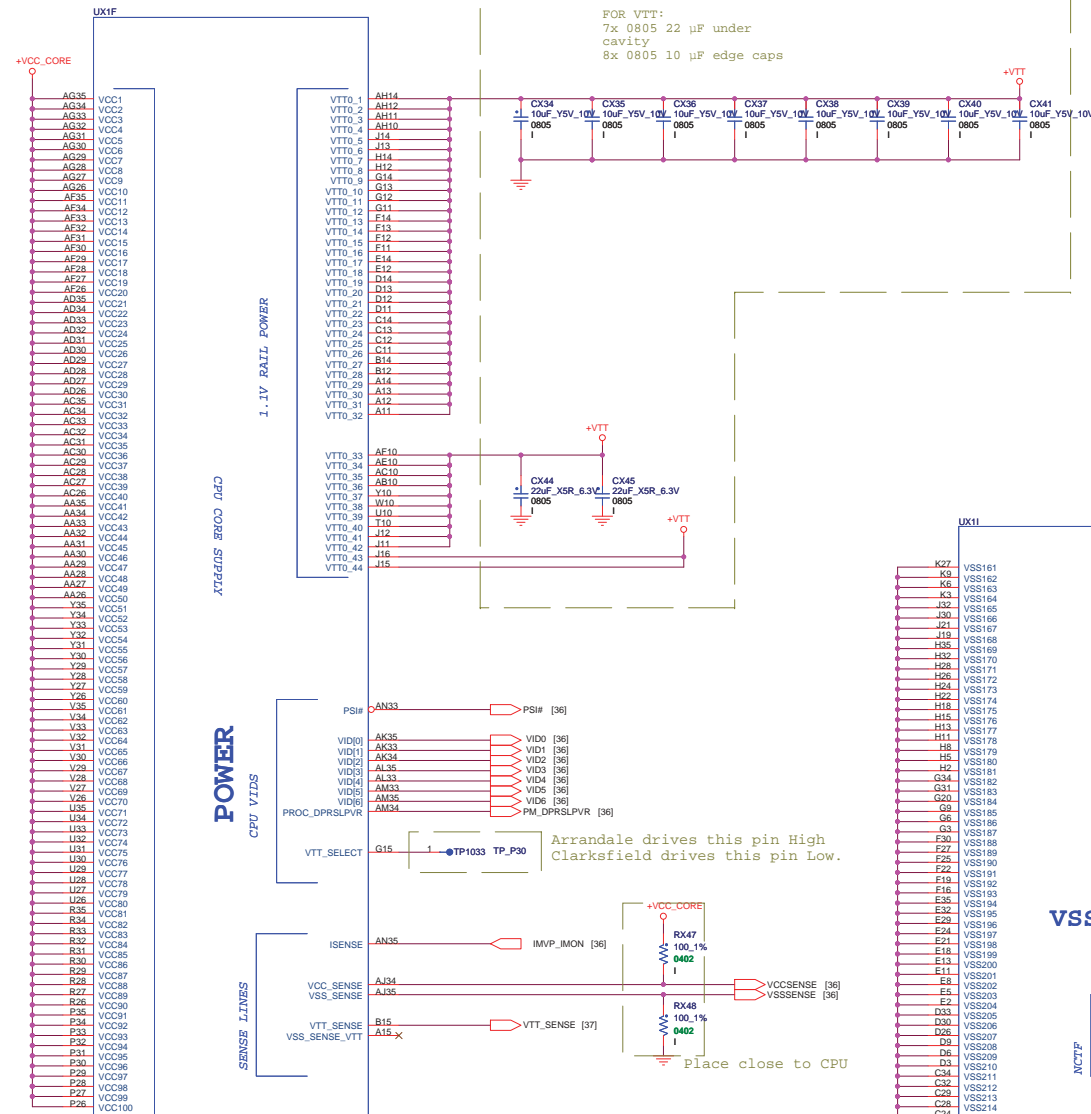
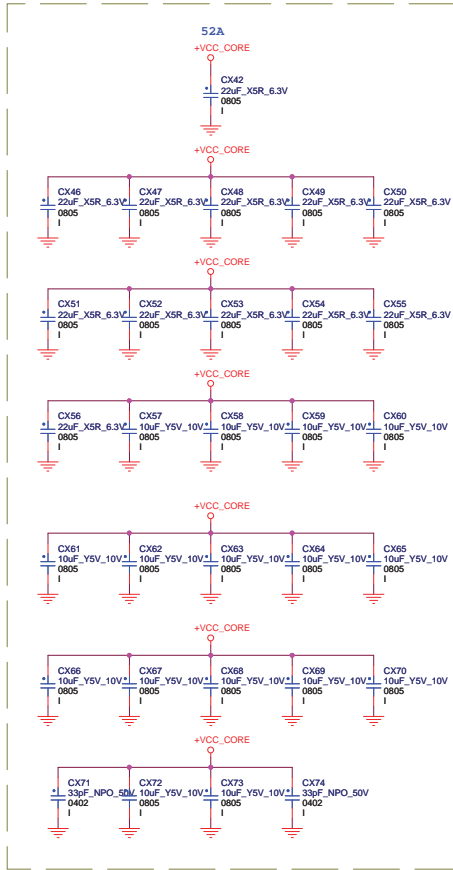
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Foxconn eMS Inc.		HNBD R&D	
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Title			
RESET SIGNAL MAP			
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Place close to chip

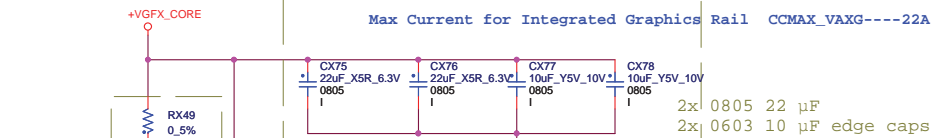


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Title Calpella (CLK,MISC,JTAG)			
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FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10 μ F
between inductor and socket on top layer



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Discrete GPU: Not Install
UMA: Install

GRAPHICS

POWER

FDI

PBG & IMT

Socket_INTEL989_15u

+VTTQ [10,12,17,18,28,36,37,40]
+VGFX_COREQ [40]
+V1.5_VDDQ [10,18,28,30,39]
+V1.8SQ [18,38,39]

Discrete GPU: Not Install
UMA: Install

Discrete GPU: Install
UMA: Not Install

Discrete GPU: Not Install
UMA: Install

DDR3 - 1.5V RAILS

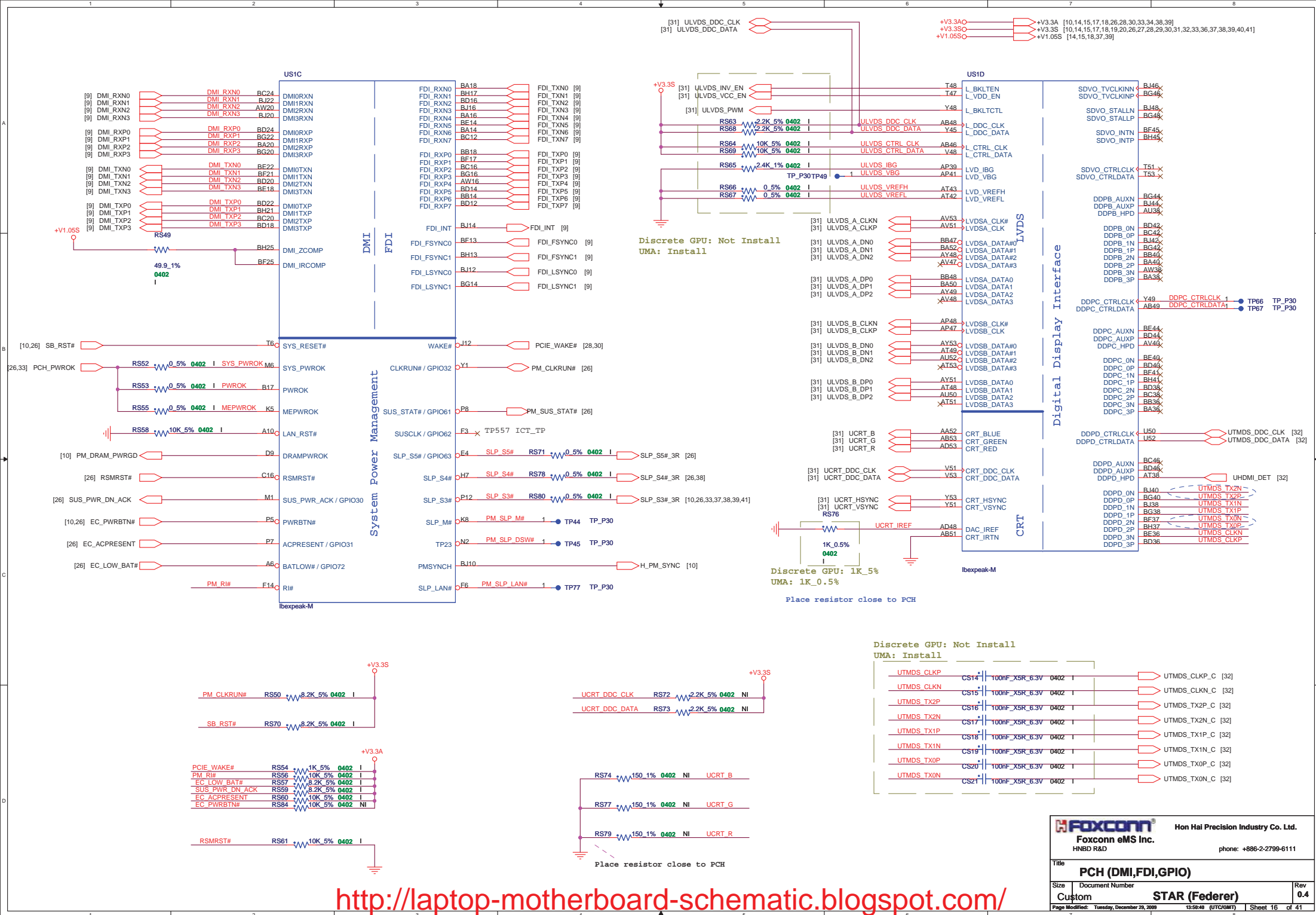
1.1V

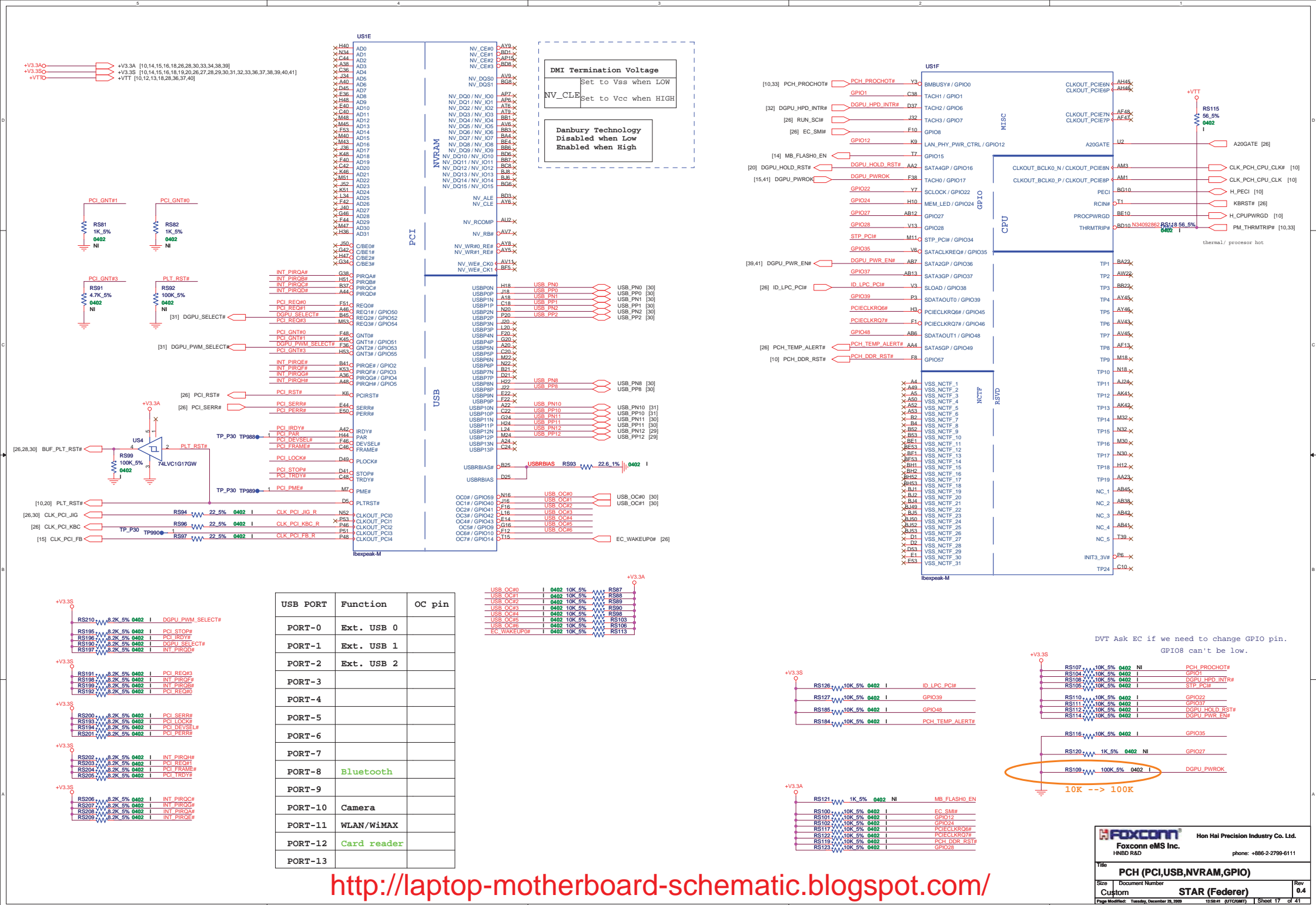
1.8V

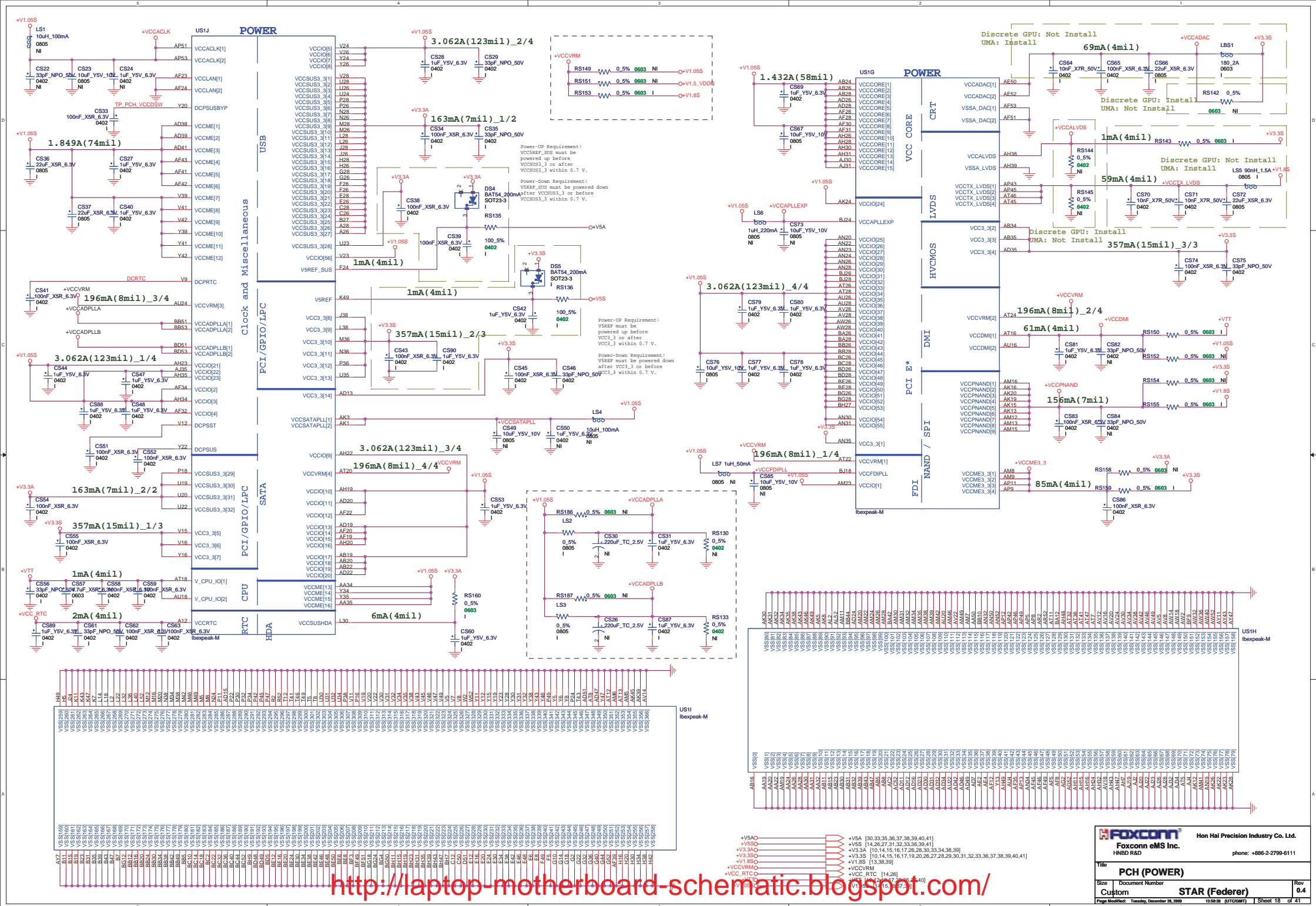
FOR VCCPLL:
1x 0805 2.2 μ F
2x 0805 1 μ F
1x 0805 22 μ F
1x 0603 4.7 μ F

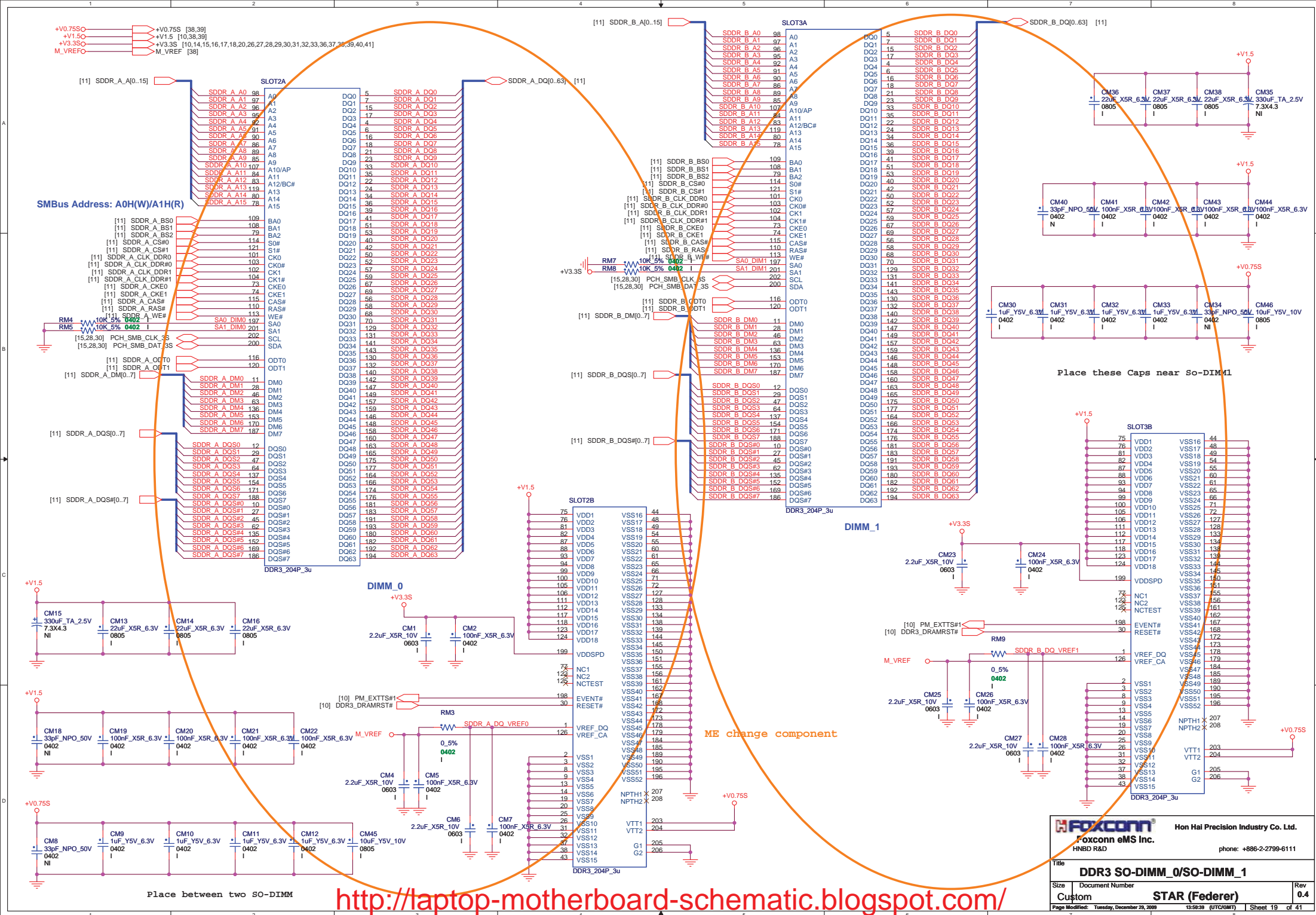
Max Current for VCCPLL Rail 1.35A

FOR DDR3:
5x 0402 1 μ F
2x 0805 22 μ F

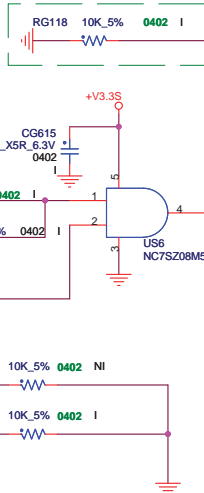








M93-S3 Not Install
PARK-S3 Install 10K ohm



If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.

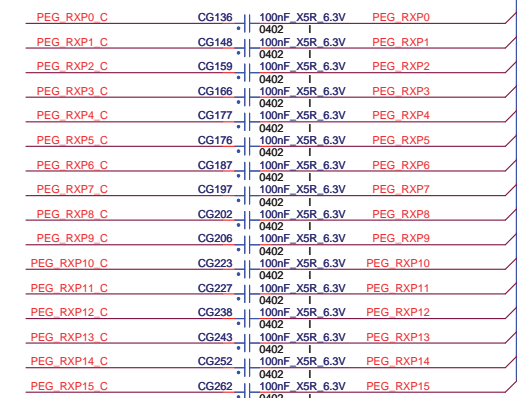
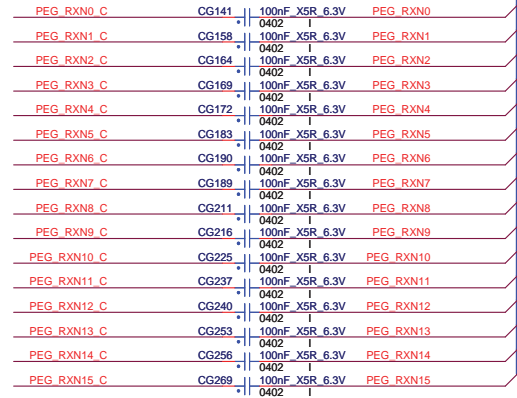
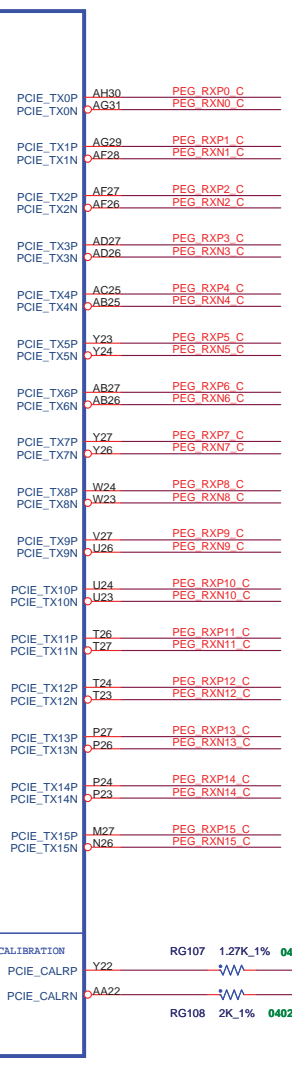
Reserved 011
512MB 001

HSYNC , VSYNC
AUD[1] , AUD[0]

0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

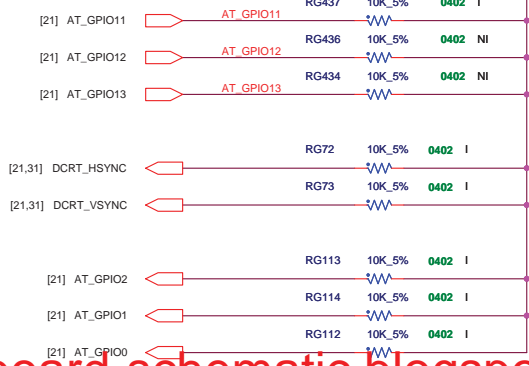
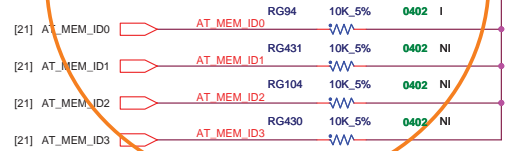
PCI EXPRESS INTERFACE



Modify setting by different VRAM vendor

Strap for DDR3
AT_MEM_ID (3:2:1:0)

0000	64Mx16	Samsung (K4W1G1646E-HC12)	512MB
0001	64Mx16	Hynix (H5TQ1G63BFR-12C)	512MB
0010	128Mx16	Samsung (K4W2G1646B-HC12)	1GB
0100	128Mx16	Samsung (K4W2G1646C-HCxx)	1GB
1000	128Mx16	Hynix (H5TQ2G63BFR-12C)	1GB
1001	128Mx16	Micron (MT41J128M16HA-12)	1GB



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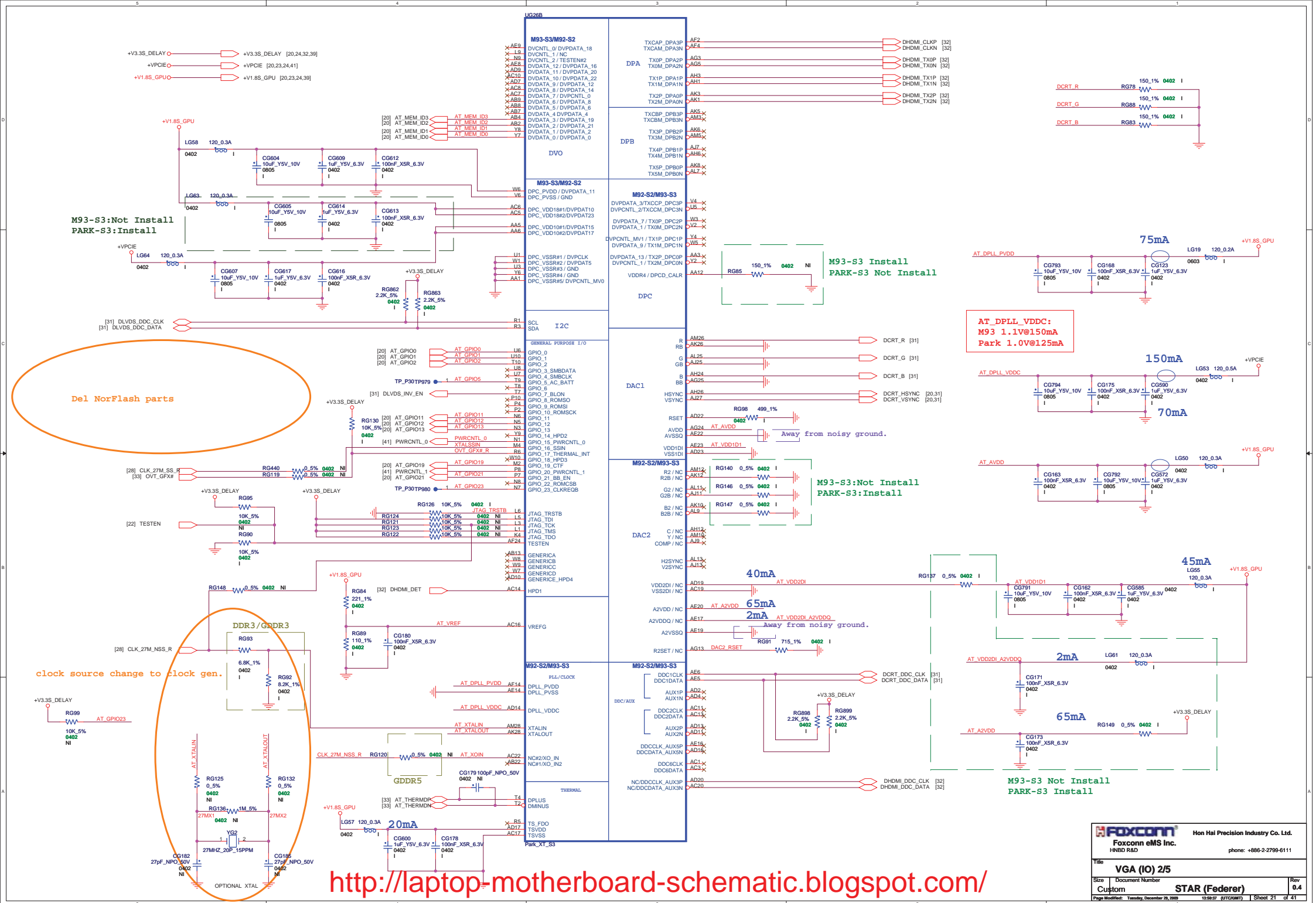
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Foxconn eMS Inc.
HNBD R&D
phone: +886-2-2799-6111

Title
VGA (PCI-E/STRAP) 1/5

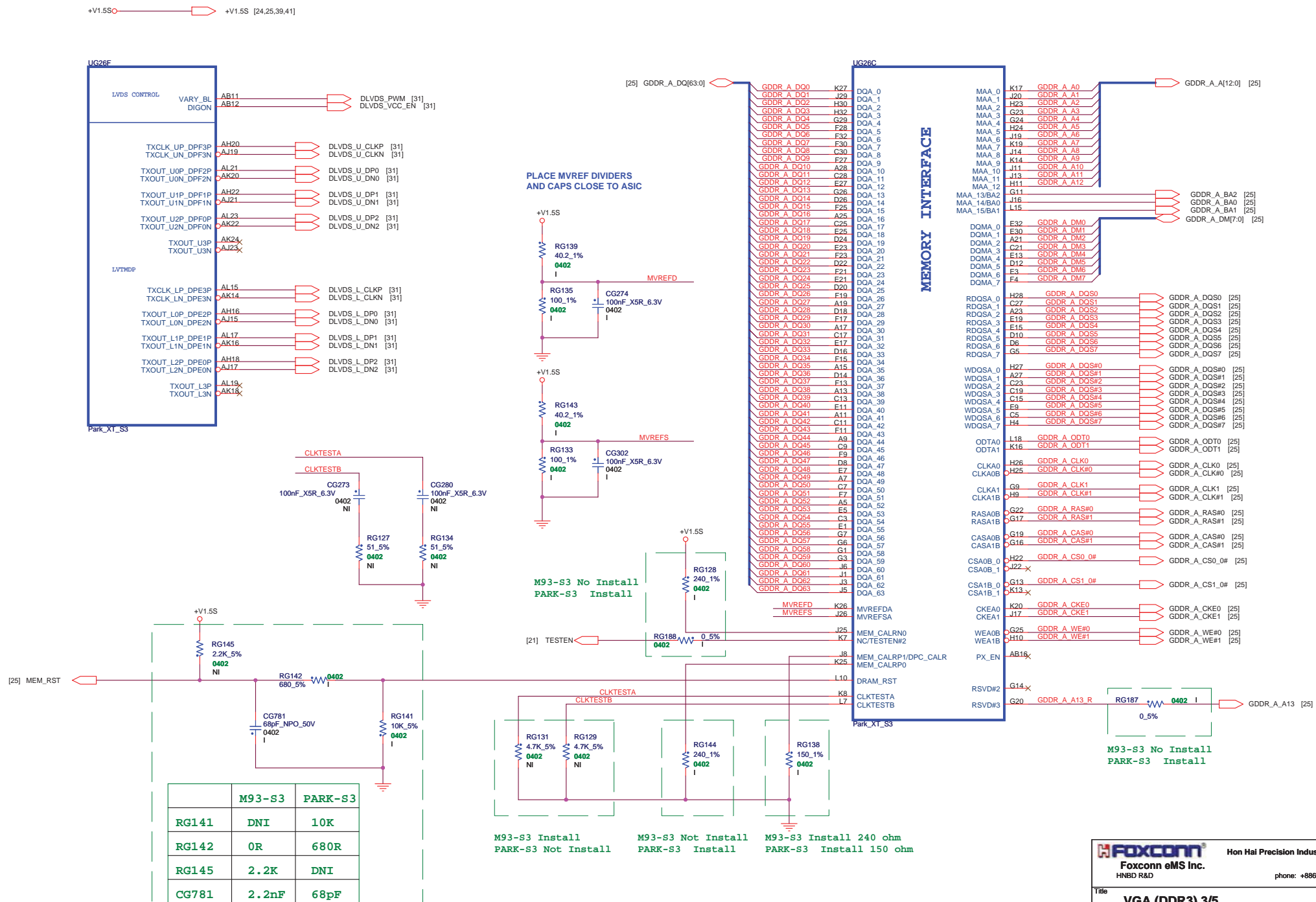
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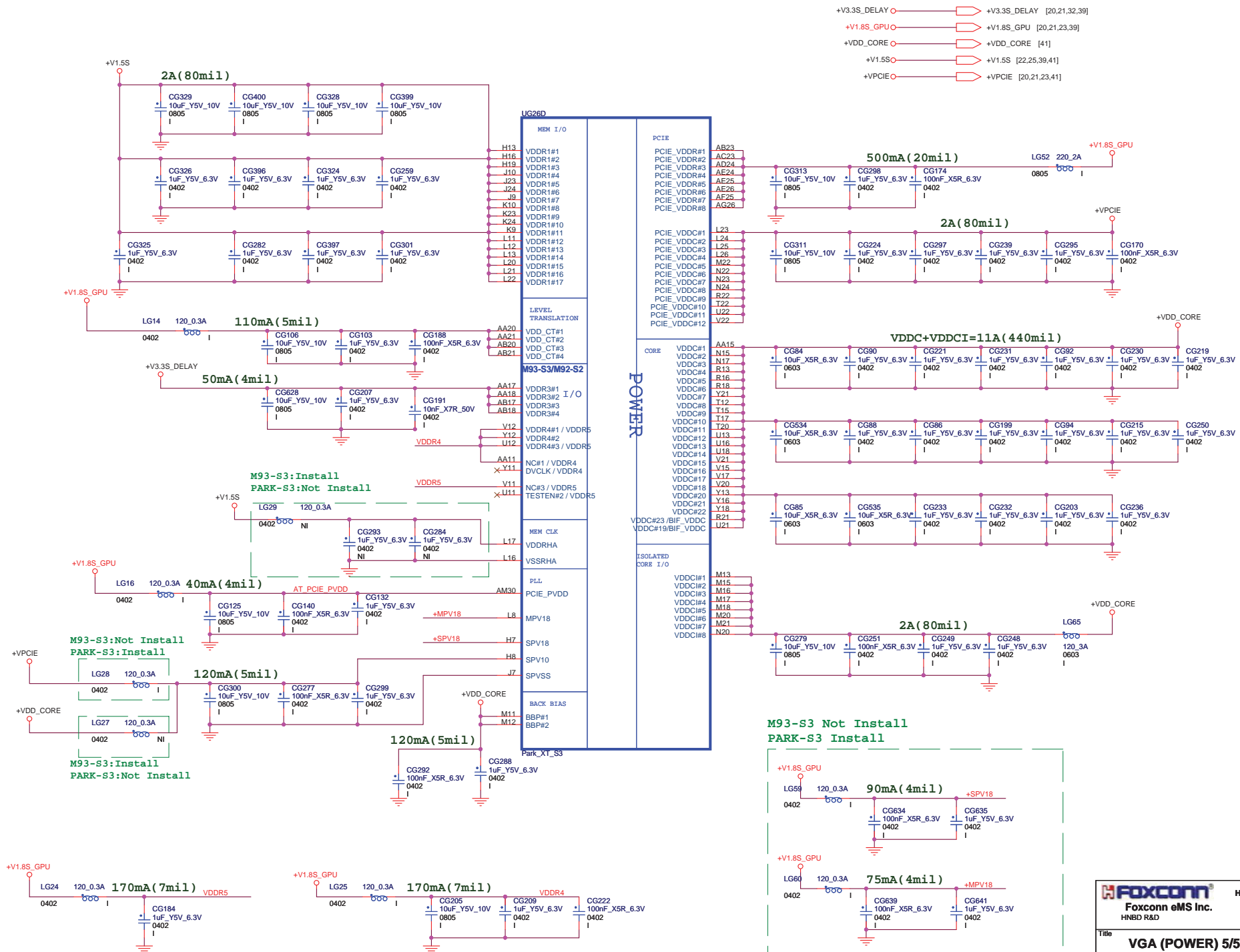
Rev
0.4

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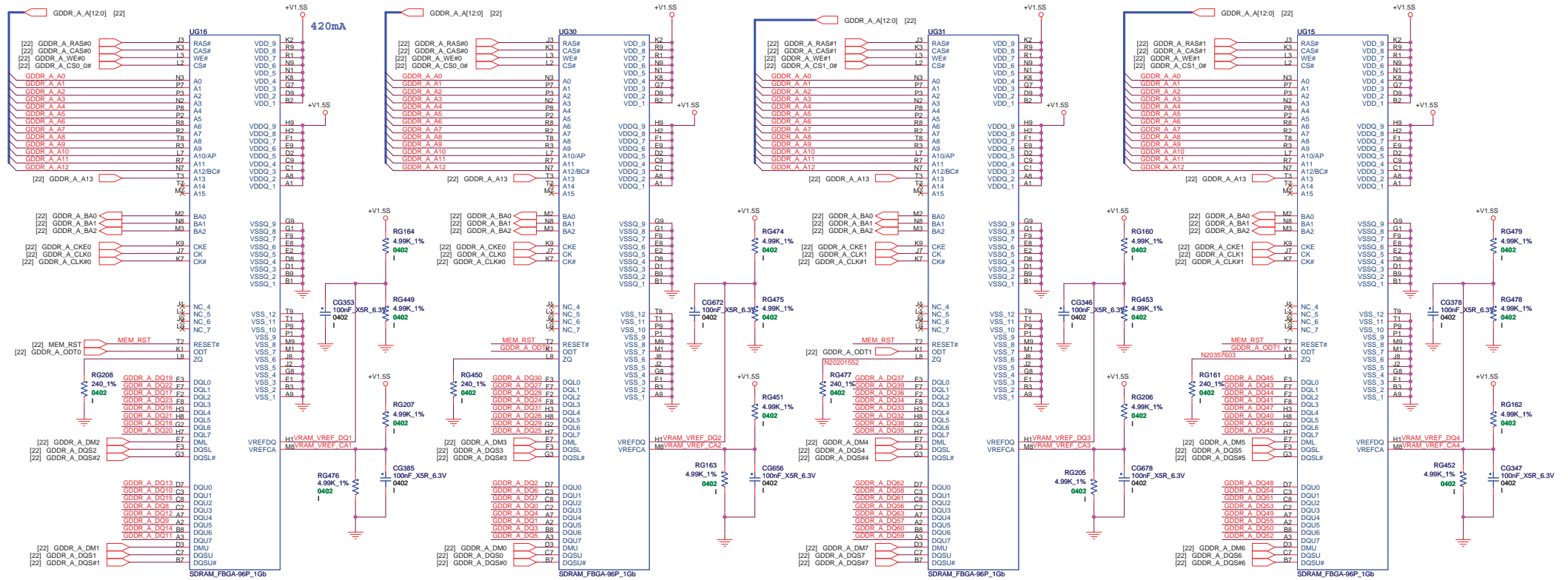
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+V1.5S

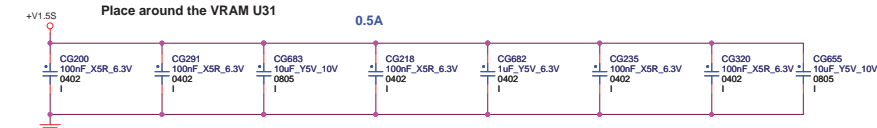
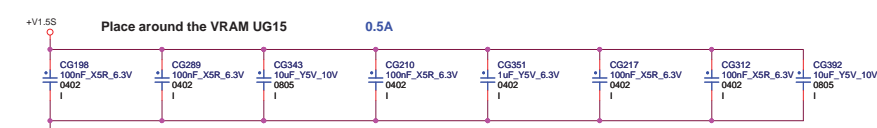
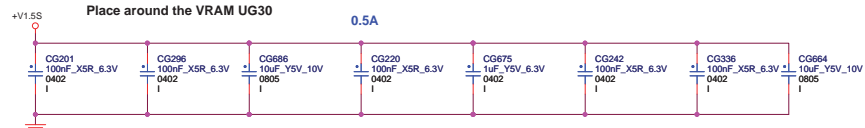
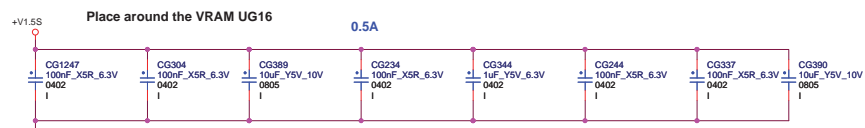


GDDR_A_DQ[0:31] [22]

GDDR_A_CLK0 56.5%
GDDR_A_CLK# 56.5%

GDDR_A_DQ[32:63] [22]

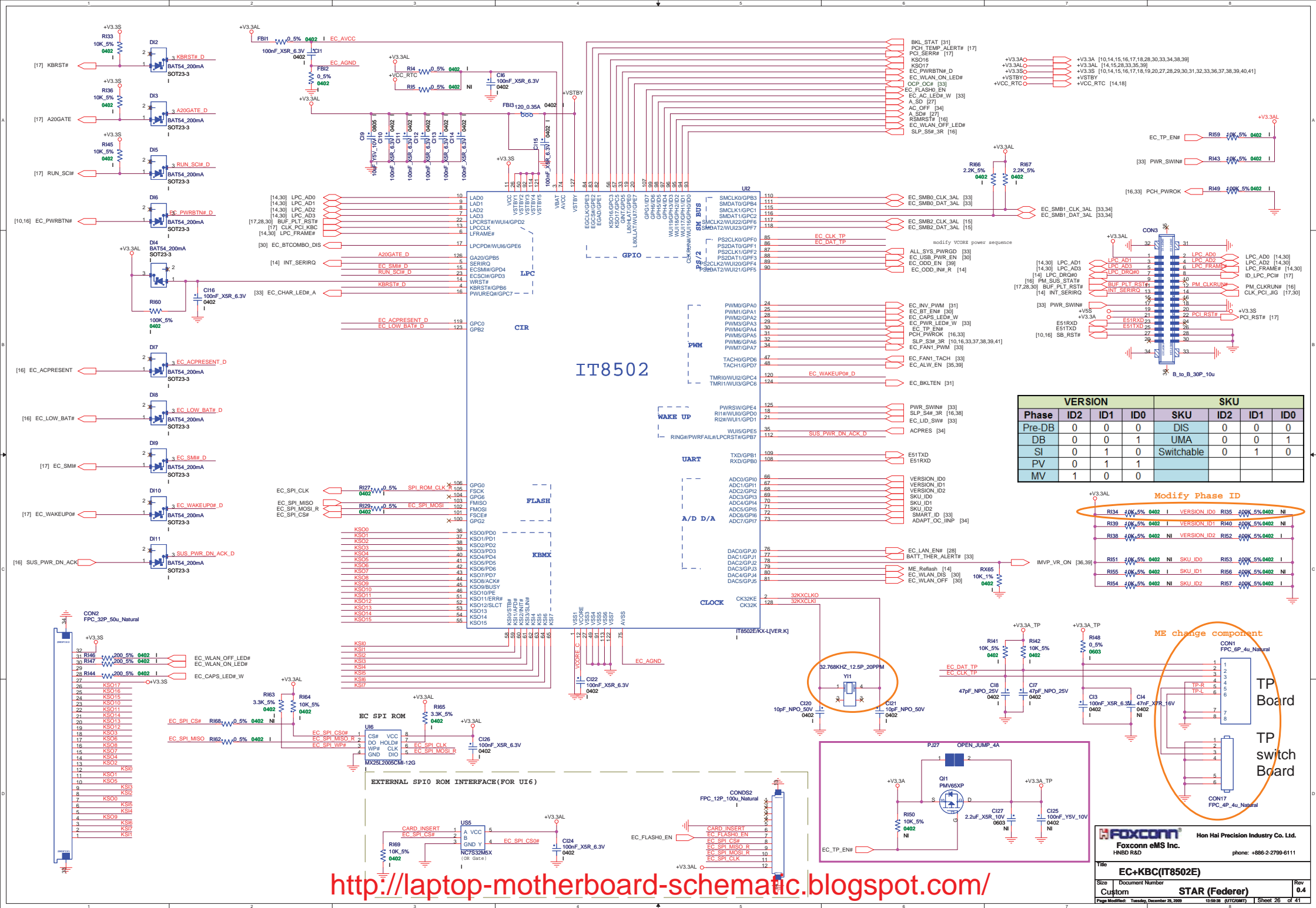
GDDR_A_CLK1 56.5%
GDDR_A_CLK# 56.5%



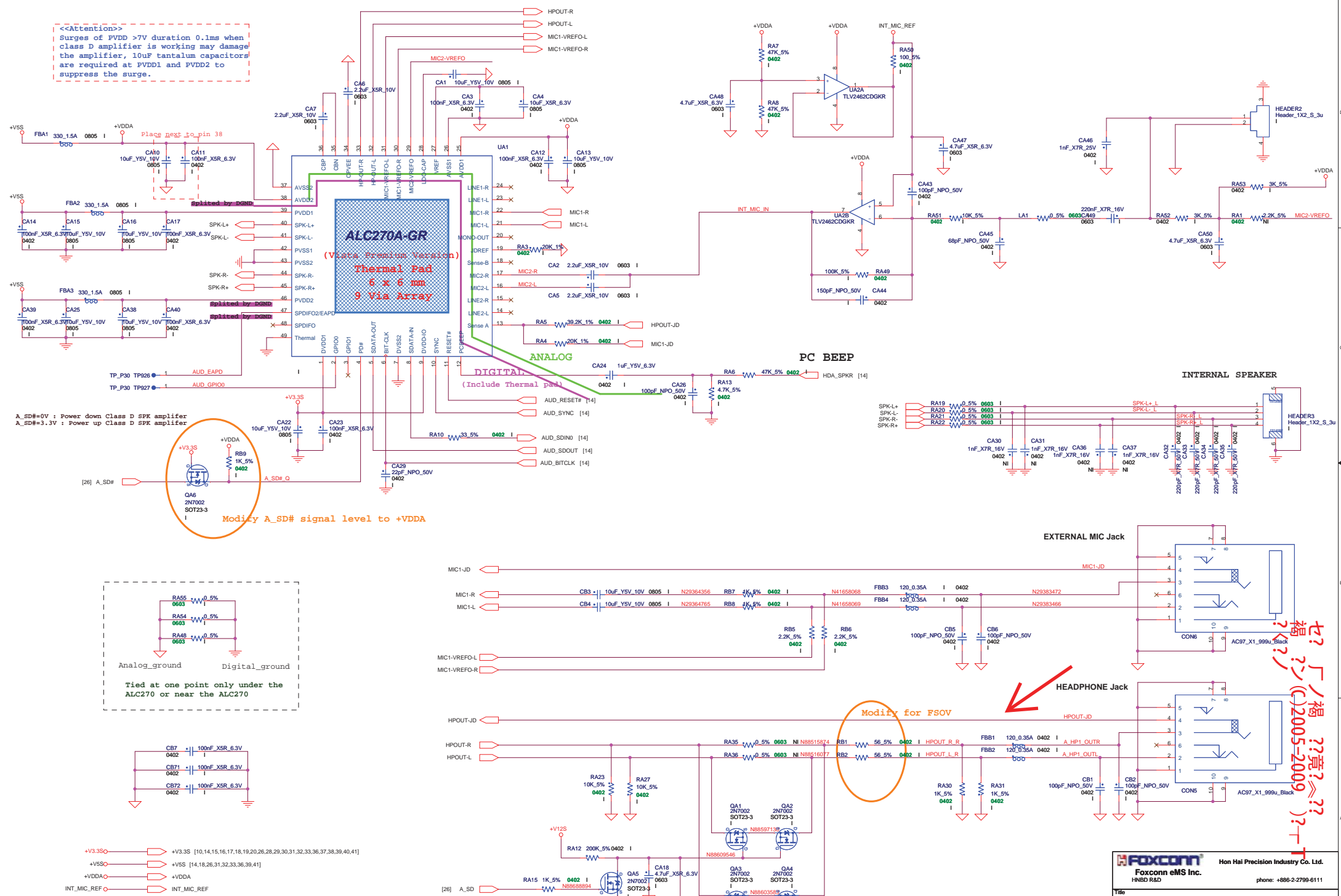
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Title			
VRAM (DDR3)			
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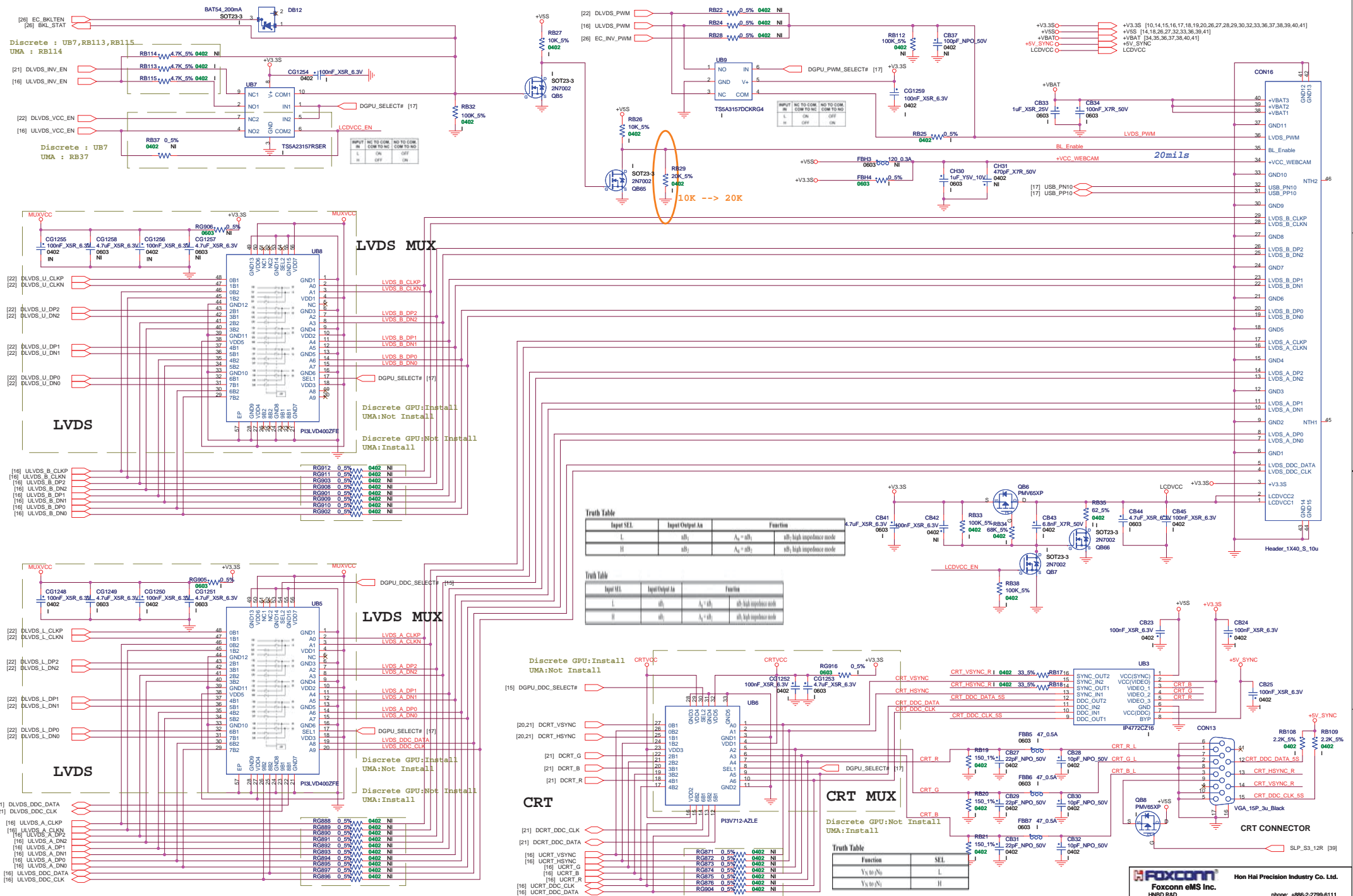
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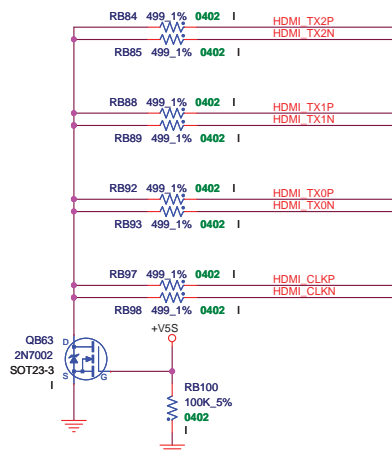
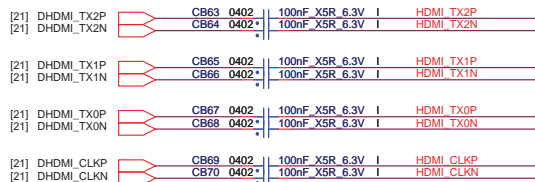
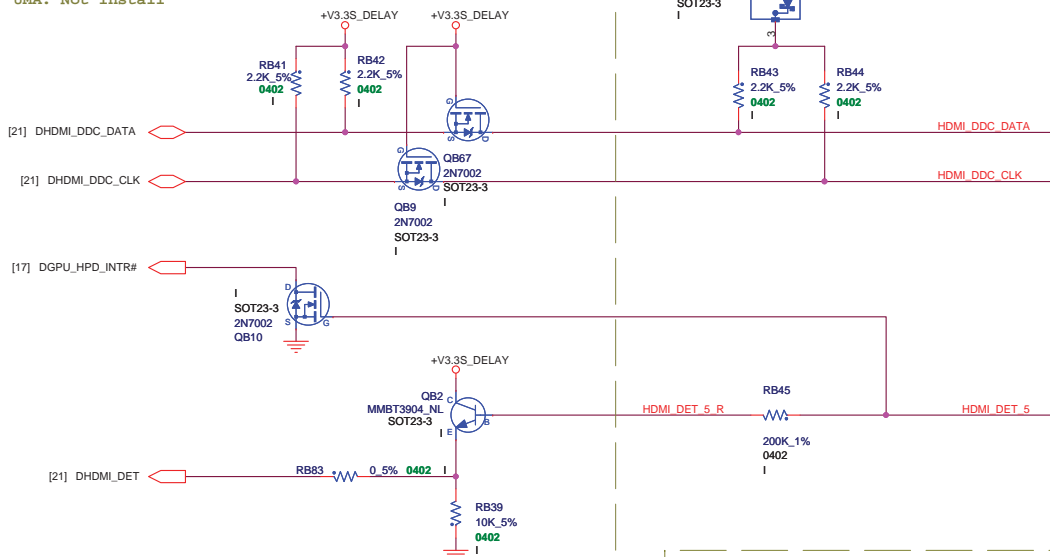


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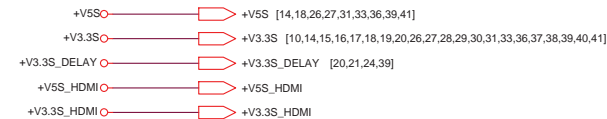
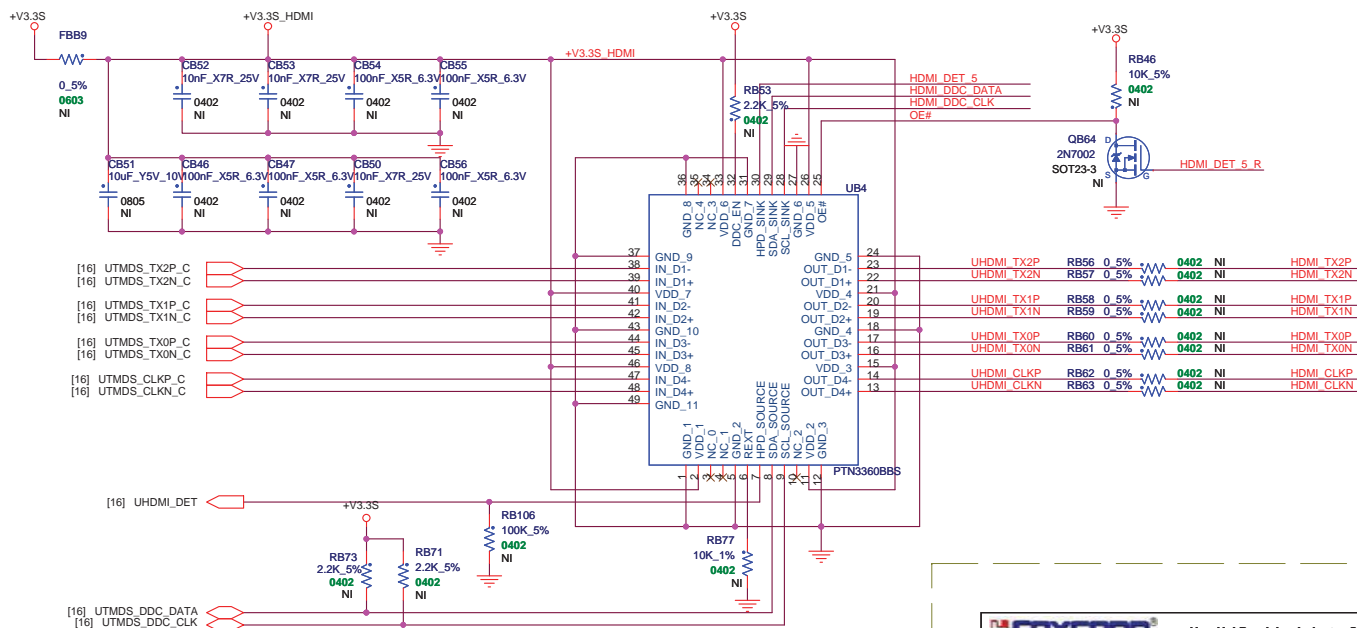


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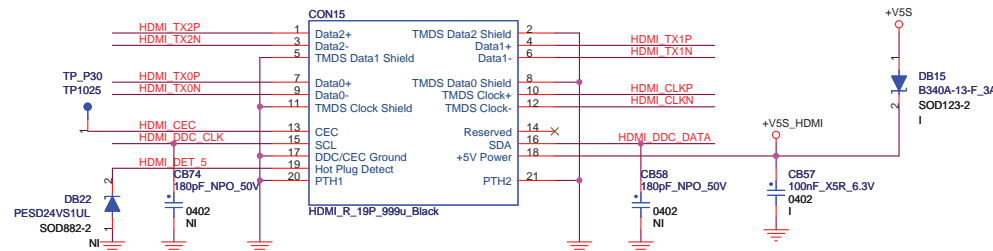
Discrete GPU: Install
UMA: Not Install



Discrete GPU:Not Install
UMA:Install

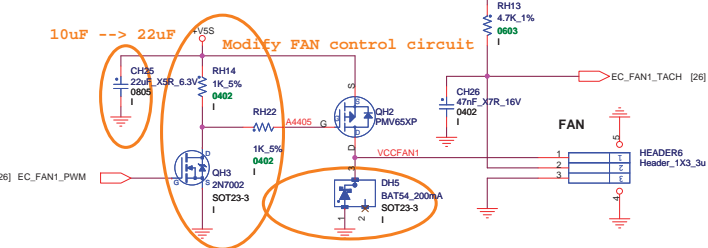


HDMI spec: +5V:4.7V min , 55mA max.

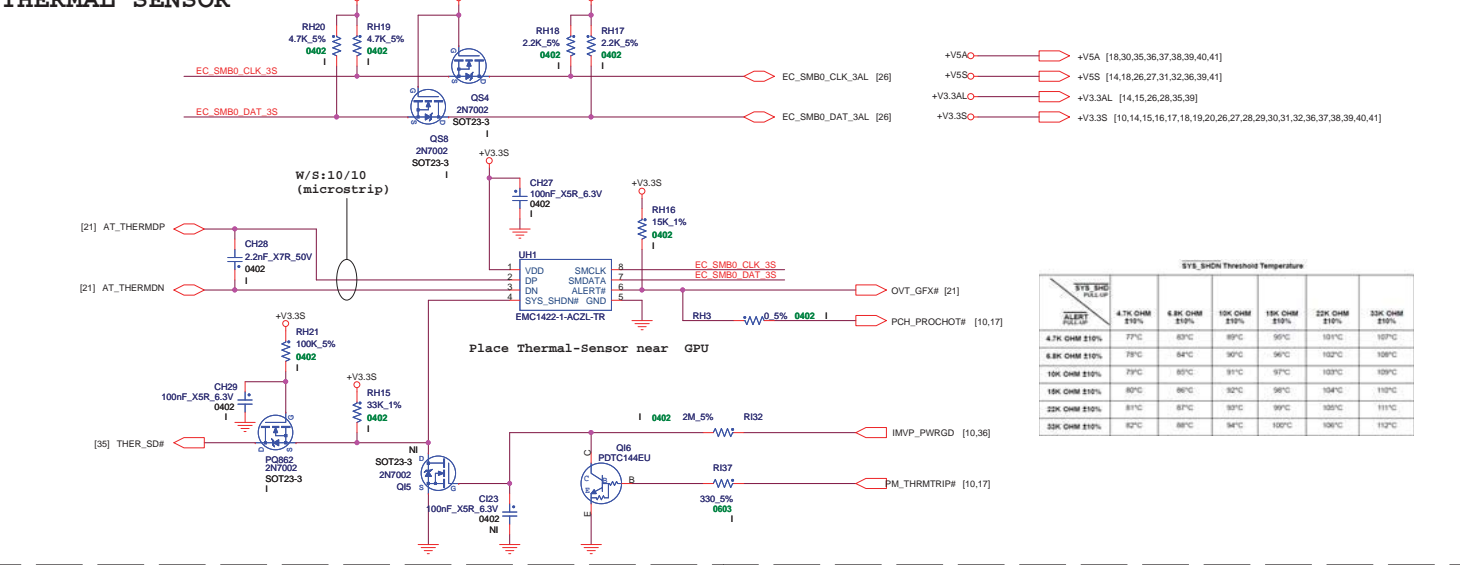


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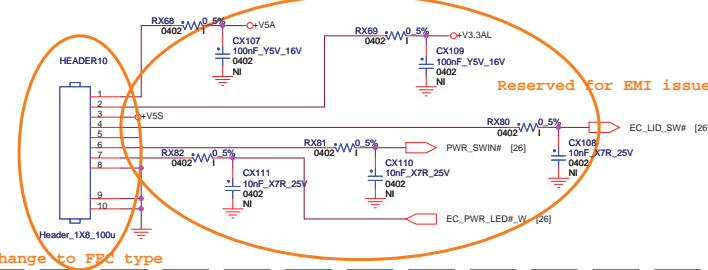
FAN CONNECTOR



THERMAL SENSOR



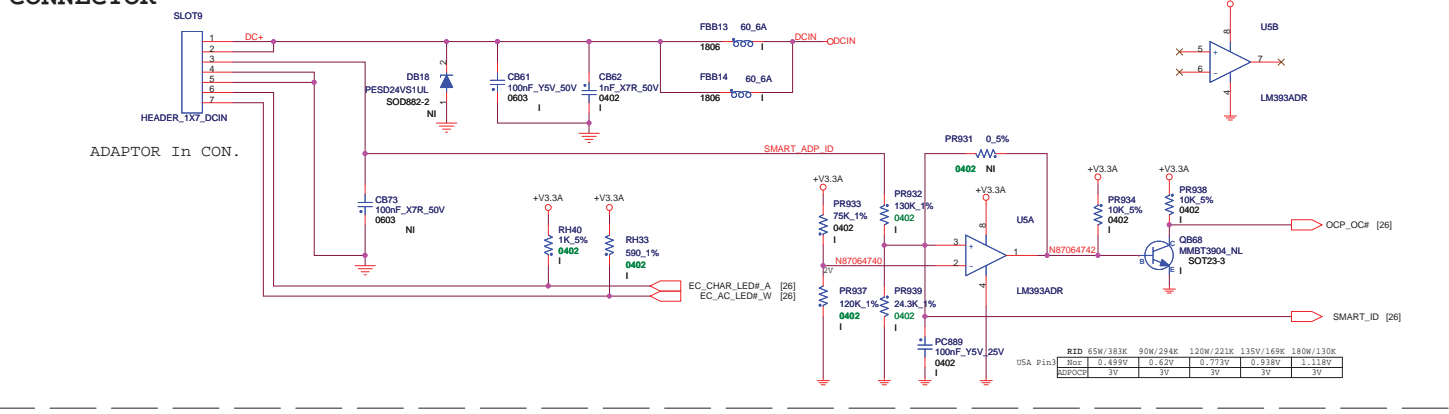
POWER BUTTON BOARD CONNECTOR



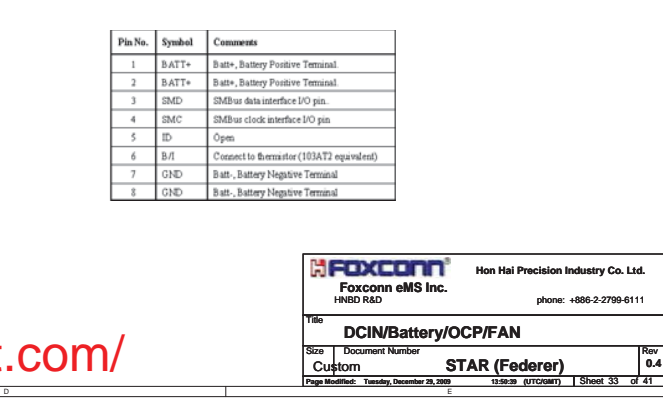
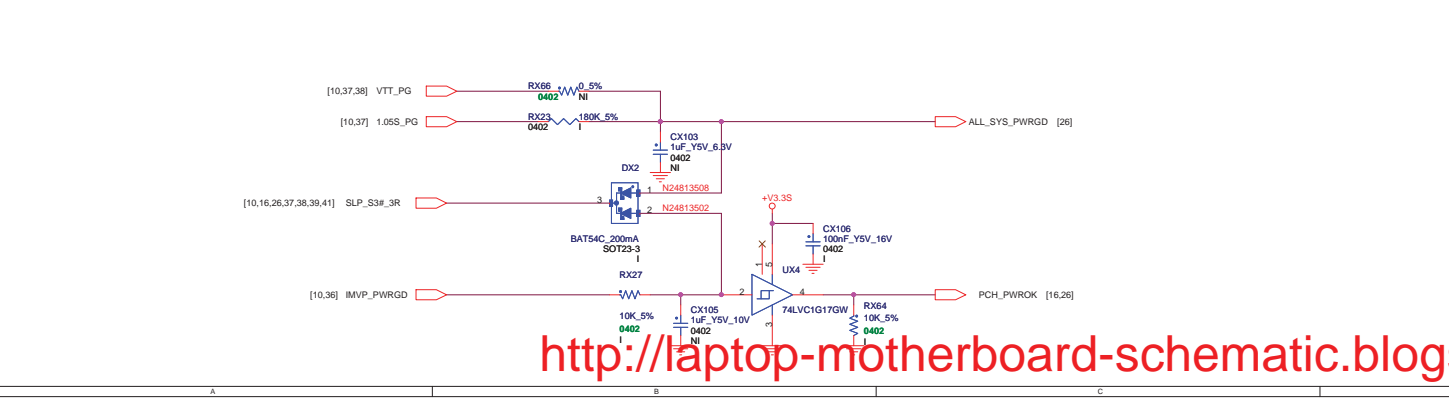
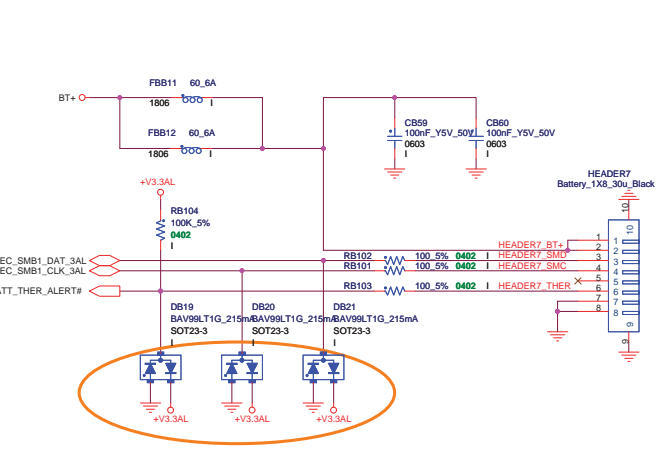
DC JACK

Wire to Board

CONNECTOR



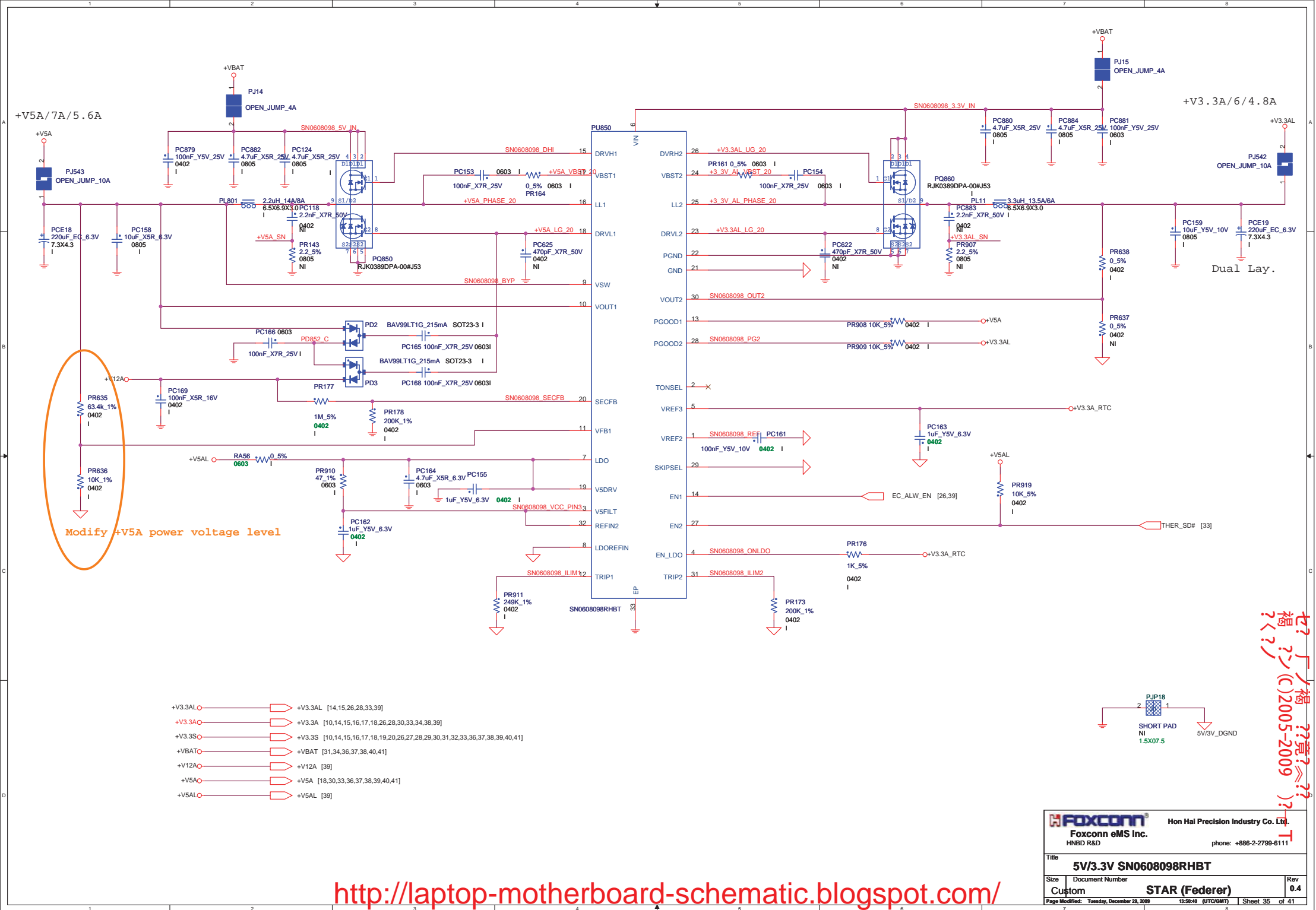
BATTERY CONNECTOR



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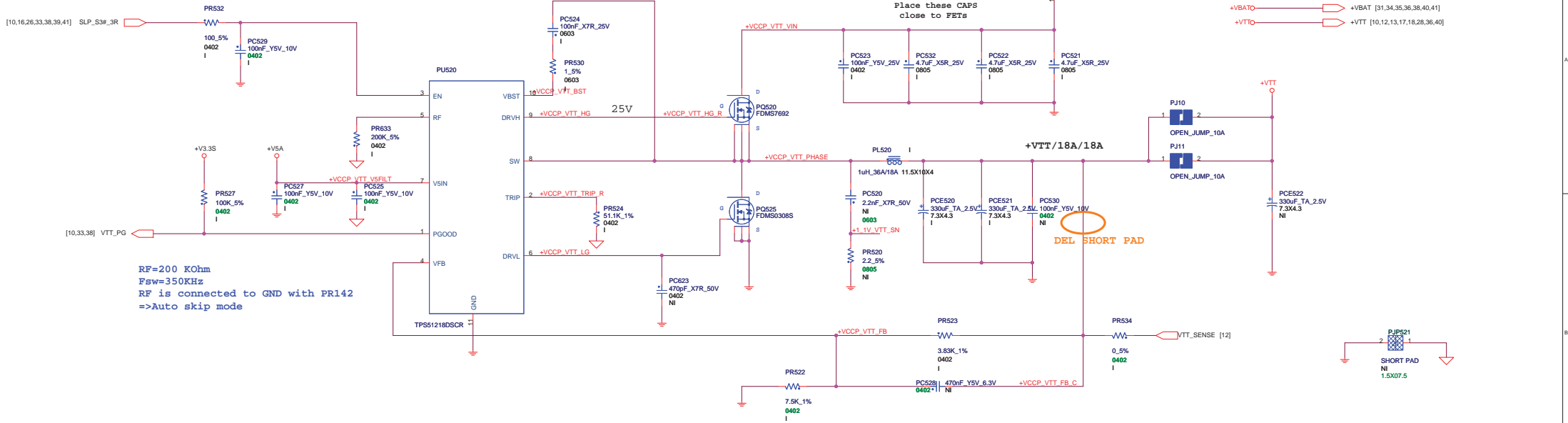
SYS_WDT PULL-UP		SYS_WDT Threshold Temperature						
4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%			
77°C	82°C	86°C	90°C	94°C	98°C			
77°C	82°C	86°C	90°C	94°C	98°C			
77°C	82°C	86°C	90°C	94°C	98°C			
80°C	86°C	90°C	94°C	98°C	102°C			
80°C	86°C	90°C	94°C	98°C	102°C			
81°C	87°C	91°C	95°C	99°C	103°C			
82°C	88°C	92°C	96°C	100°C	104°C			

Pin No.	Symbol	Comments
1	BATT+	Batt., Battery Positive Terminal
2	BATT+	Batt., Battery Positive Terminal
3	SMD	SMBus data interface I/O pin.
4	SMC	SMBus clock interface I/O pin.
5	ID	Open
6	B/I	Connect to terminator (10kΩ equivalent)
7	GND	Batt., Battery Negative Terminal
8	GND	Batt., Battery Negative Terminal

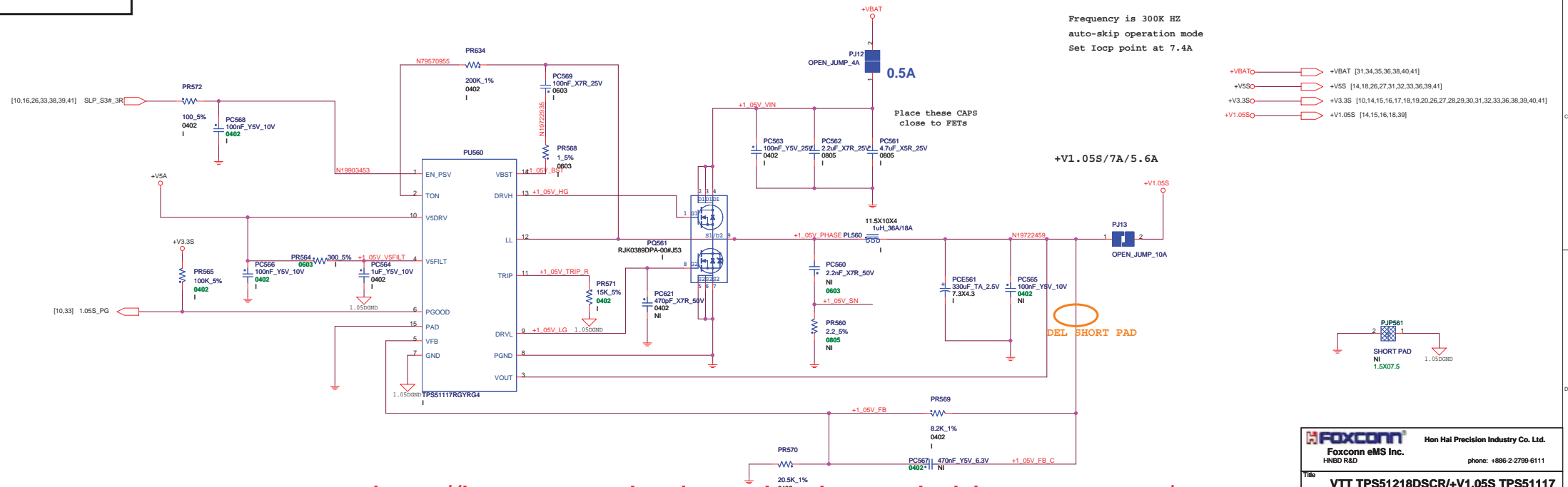




+VTT TPS51218



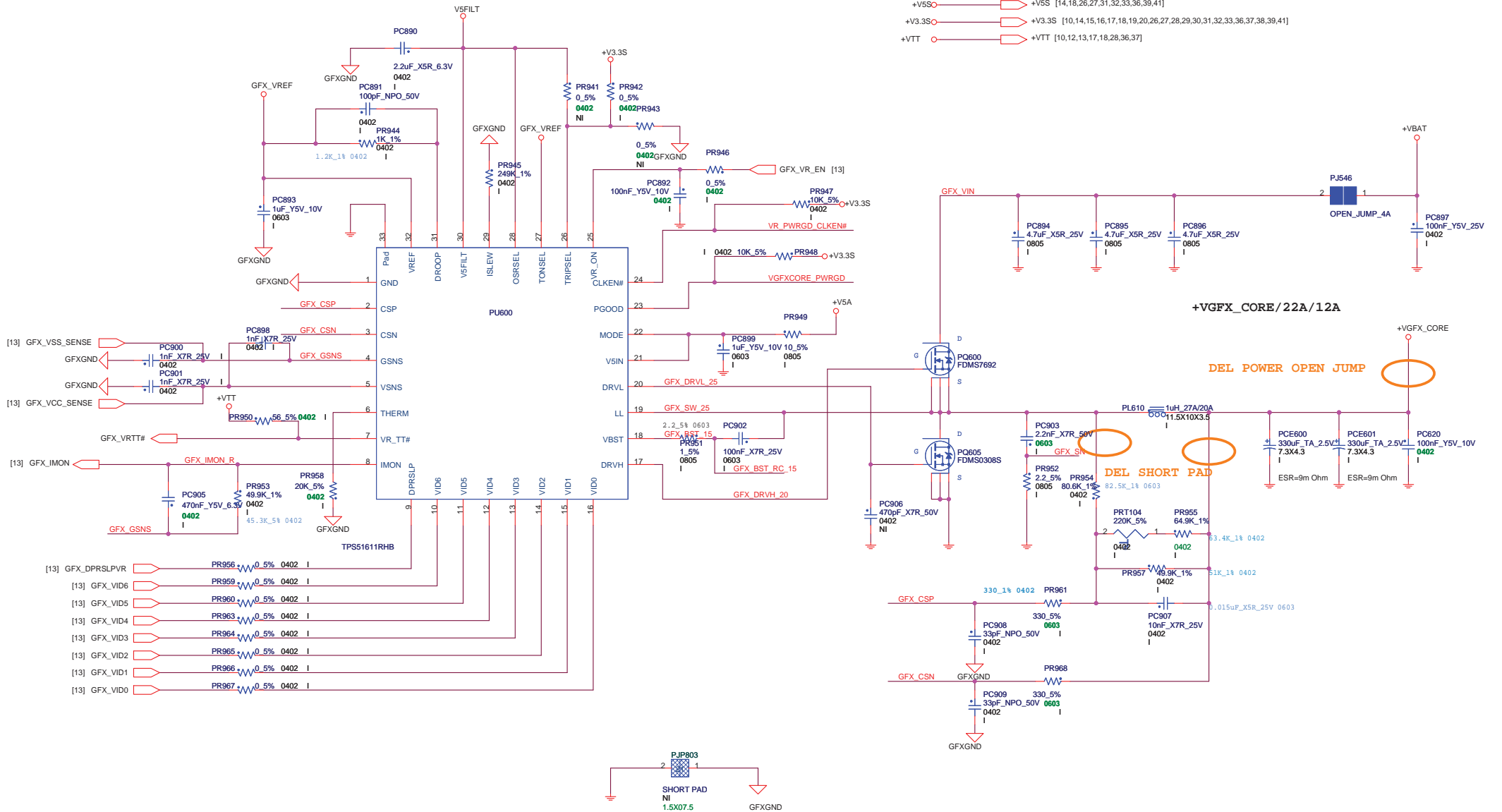
+V1.05S TPS51117

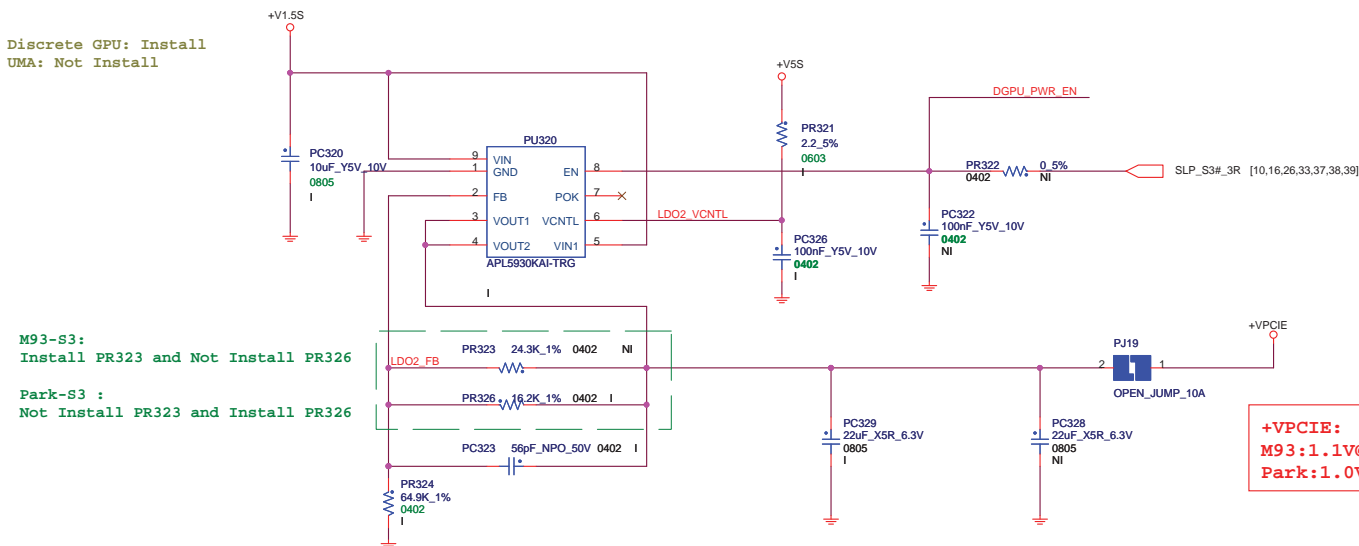
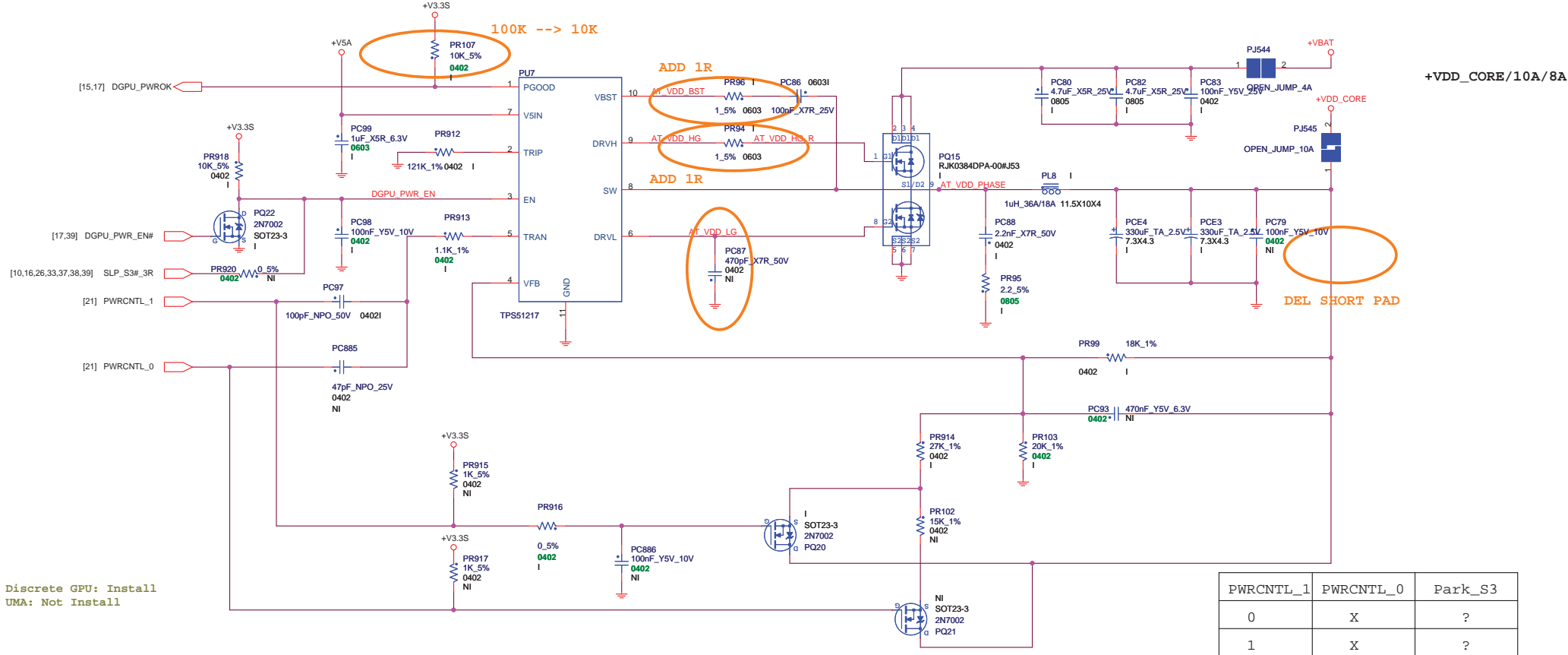


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+VGFXCORE





- +VBAT → +VBAT [31,34,35,36,37,38,40]
- +V5A → +V5A [18,30,33,35,36,37,38,39,40]
- +V5S → +V5S [14,18,26,27,31,32,33,36,39]
- +V3.3S → +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40]
- +V1.5S → +V1.5S [22,24,25,39]
- +VDD_CORE → +VDD_CORE [24]
- +VPCIE → +VPCIE [20,21,23,24]

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